1991

Design of an ISDN central office, U-interface

Timothy N. Toillion
Iowa State University

Design of an ISDN central office, U-interface

by

Timothy N. Toillion

A Thesis Submitted to the

Graduate Faculty in Partial Fulfillment of the

Requirements for the Degree of

MASTER OF SCIENCE

Department: Electrical Engineering and Computer Engineering
Major: Computer Engineering

Signatures have been redacted for privacy

Signatures have been redacted for privacy

Iowa State University
Ames, Iowa
1991

TABLE OF CONTENTS

INTRODUCTION 1

CHAPTER 1. THE EVOLUTION OF TELECOMMUNICATIONS 4

Telephone Communications 4

Inventions Spawn Growth 4

Modern Telecommunication Networks 8

Telecommunications 11

Definition of Telecommunication 11

Other Forms of Telecommunication 11

Integration of Services 12

Evolution of the Concept 12

The Evolution of ISDN 15

CCITT's Standards 15

Major Setback 16

Evolution of Products and Services 16

CHAPTER 2. ISDN 18

Services 18

Functional Architecture 20

Standards 22

CCITT I-Series Recommendations 22
ISDN Reference Model 23
The Physical Layer 25
Specified Functions 25
Transmission Rates 26
User-Interface Rates 26
Reference Point Signaling Standards 28
The Data Link Layer 30
LAP-D: The D Channel Interface 31
LAP-B: The B Channel Interface 32
The Network Layer 33
CHAPTER 3. THE ORIGINAL CENTRAL OFFICE DESIGN . . 35
Goals 35
The PC Card 36
The MITEL ST-BUS 38
ST-BUS Timing Generation 39
The PC Bus Interface 41
The Primary Rate Interface 42
The MT8980D Digital Crosspoint Switch 43
The U-Interface Components 47
MITEL's MT8972B Digital Network Interface Circuit 49
The HDLC Protocol Controller: MT8952 54
The U-Interface Design 64
Testing the PC Board 66

CHAPTER 4. THE REVISED DESIGN OF THE CENTRAL OFFICE 67

Project Goals 67

Revised Goals 67

Added Goals 68

Division of the Design Project 68

Typical Operation of a Central Office 69

Possible Connections 69

Interactions 70

Overview of the Hardware Design 71

The Main Switch Card 72

The External Board 73

The S/T-Interface Card 74

The MT8930 Subscriber Network Interface Circuit 75

SNIC Interrupt Control 77

S/T-Card Memory Mapping 77

The Microprocessor System 78

CHAPTER 5. THE DETAILED DESIGN OF THE U-INTERFACE PC BOARD 79

General Hardware Design Changes 79

U-Interface Operation 80

Component Interaction Changes 80

Additional Functionality 81

INTEL 8254 Programmable Interval Timer 81

Operation 82
Initialization 82
The ST-BUS Interface 83
The 26 Pin Ribbon Connector 83
The Interface Circuit 84
The PC-BUS Interface 84
The PC-BUS Pin Assignments 84
IDT 7130SA/LA Dual-Port RAM 84
Supporting Circuits 86
The Microprocessor System 87
The MC6809 87
Memory 90
PAL Chip Select 90
CONCLUSION 94
Status of the ISDN Central Office Project 94
Interface Capabilities 94
Commercial Schematics 94
U-Interface Card Testing 95
Suggested Design Changes 96
The U-Interface Card 96
BIBLIOGRAPHY 99
APPENDIX A. ACRONYMS 101
APPENDIX B. CCITT I-SERIES RECOMMENDATIONS 105

I.100 Series: General Structure 105
Section 1: Frame of I-Series Recommendations - Terminology 105
Section 2: Description of ISDNs 105
Section 3: General Modeling Methods 105
Section 4: Telecommunication Network and Service Attributes 105
I.200 Series: Service Capabilities 106
Section 1: Service Aspects of ISDNs 106
Section 2: Common Aspects of Services in an ISDN 106
Section 3: Bearer Services Supported by an ISDN 106
Section 4: Teleservices Supported by an ISDN 106
Section 5: Supplementary Services in an ISDN 106
I.300 Series: Overall Network Aspects and Functions 107
Section 1: Network Functional Principles 107
Section 2: Reference Models 107
Section 3: Numbering, Addressing, and Routing 107
Section 4: Connection Types 107
Section 5: Performance Objectives 107
I.400 Series: ISDN User-Network Interfaces 108
Section 1: ISDN User-Network Interfaces 108
Section 2: Application of I-Series Recommendations to ISDN User-Network Interfaces 108
Section 3: ISDN User-Network Interfaces: Layer 1 Recommendations 108
Section 4: ISDN User-Network Interfaces: Layer 2 Recommendations 108
Section 5: ISDN User-Network Interfaces: Layer 3 Recommendations 108

Section 6: Multiplexing, Rate Adaptation, and Support of Existing Interfaces 109

Section 7: Aspects of ISDN Affecting Terminal Requirements 109

I.500 Series: Internetworking Between Various Networks 109

I.600 Series: Maintenance Principles 110

A.2: OTHER RECOMMENDATIONS RELATED TO ISDN 110

APPENDIX C. U-CARD COMPONENT PIN ASSIGNMENTS . . 111

APPENDIX D. PARTS LISTS 121

Main Card Parts List 121

U-Interface Card Parts List 121

External Board Parts List 121

APPENDIX E. PAL AND CIRCUIT TEST PROGRAMMING . . 126

PAL Programming and Generated Files 126

PAL Program 126

PAL JED File 127

PAL Plot File 128

Circuit Test Programs 129

SRAM and EPROM Pin Test 129

DP-RAM Test 129

Switch, Controller, Timer and HDLC Interrupt Test 130

Daisy-Chain DNIC and Interrupt Tests 133

APPENDIX F. U-CARD SCHEMATICS 138

Gate to Chip Schematics 138

PC Board Schematics 138

LIST OF TABLES

Table 1.1: CCITT Study Groups 14

Table 2.1: Possible ISDN Services and User Applications 19

Table 2.2: ISDN Channel Types 26

Table 2.3: D-Channel Contention Priority Assignment 29

Table 3.1: MT8980D Connection Memory Bits 46

Table 3.2: MT8980D Control Register Bits 46

Table 3.3: MT8972B Mode Definitions 50

Table 3.4: MT8972B Status Register 51

Table 3.5: MT8972B Control Register 53

Table 3.6: MT8972B Diagnostic Register 54

Table 3.7: MT8952 Register Addresses 57

Table 3.8: MT8952 FIFO: Received Byte Status 58

Table 3.9: MT8952 FIFO: Receive FIFO Status 58

Table 3.10: MT8952 FIFO: Transmit FIFO Status 59

Table 3.11: MT8952 General Status Register Bit Definitions 59

Table 3.12: MT8952 Interrupt Flag Register 60

Table 3.13: MT8952 Control Register Bit Definitions 60

Table 3.14: MT8952 Timing Control Register 61

Table 5.1: 8254 Interval Timer Control Register 82

Table 5.2: The MC6809 Condition Code Register 89

Table C.1: MT8910 DSLIC Pin Assignments 112

Table C.2: MT8952B HDLC Protocol Controller Pin Assignments 113

Table C.3: MT8972 DNIC Pin Assignments 114

Table C.4: The MT8980 DX Pin Assignments 115

Table C.5: Motorola 6809 Microprocessor Pin Assignments 116

Table C.6: The 64k Byte EPROM Pin Assignments 117

Table C.7: The 8k Byte SRAM Pin Assignments 118

Table C.8: The 1k Byte Dual-Port RAM Pin Assignments 119

Table C.9: The 8254 Interval Timer Pin Assignments 120

Table D.1: Main Card Components 122

Table D.2: S/T-Card Components 123

Table D.3: U-Card Components 124

Table D.4: External Components 125

LIST OF FIGURES

Figure 1.1: Alexander Graham Bell's Telephone 4

Figure 1.2: Early Service and Switchboard Service 5

Figure 1.3: Automatic Two Phase Switches 6

Figure 1.4: An Early Wall Phone 7

Figure 1.5: Telephone Network Switching Hierarchy 9

Figure 1.6: U.S. Telecommunication Multiplexing Hierarchies 13

Figure 1.7: CCITT's Recommendations 15

Figure 1.8: Application Bandwidth Requirements 17

Figure 2.1: Conceptual View of ISDN Services to User-Interface 18

Figure 2.2: ISDN User-Interfaces 20

Figure 2.3: ISDN Reference Model 23

Figure 2.4: ISO/OSI Model Interlayer Communication 24

Figure 2.5: ISDN User-Interface Transmission Rates 27

Figure 2.6: ISDN Multi-point, Passive Bus Configuration 28

Figure 2.7: ISDN S/T-Interface Bitstream Format 29

Figure 2.8: ISDN U-Interface Bitstream Format 30

Figure 2.9: LAP-D Frame Format 31

Figure 2.10: LAP-B Frame Format 32

Figure 3.1: The Original ISU Central Office Hardware Design 37
Figure 3.2: The ST-BUS BRI Channels and Timing 38
Figure 3.3: The ST-BUS Clock Signal Generation Diagram 40
Figure 3.4: PC-Bus Interface Block Diagram 41
Figure 3.5: ST-BUS Channels at the PRI 43
Figure 3.6: The MT8980D Functional Block Diagram 44
Figure 3.7: C-Channel DNIC Control Routing 48
Figure 3.8: Line Signaling Waveforms 52
Figure 3.9: The MT8952 Functional Block Diagram 56
Figure 3.10: DNIC Daisy-Chain Diagram 64

Figure 4.1: Central Office Block Diagram 71
Figure 4.2: The Main Switch Card Block Diagram 72
Figure 4.3: The External Board Block Diagram 73
Figure 4.4: The T-Interface Card Block Diagram 74
Figure 4.5: S/T Card Memory Mapping Diagram 78

Figure 5.1: The U-Card Block Diagram 79
Figure 5.2: The ST-BUS Interface Block Diagram 83
Figure 5.3: PC-BUS Pin Assignments 85
Figure 5.4: The PC-BUS Interface Block Diagram 86
Figure 5.5: MC6809 Registers 88
Figure 5.6: U-Card Memory Mapping 91
Figure 5.7: MT8972 DNIC Block Diagram 92

Figure 5.8: MT8910 DSLIC Block Diagram 93

Figure F.1: U-Card Latch and Other Logic 139

INTRODUCTION

ISDN is an evolving global networking concept to provide a variety of services using a standard user interface over a common communication medium, namely the existing telecommunications system. Presently, separate lines are needed to provide services such as coaxial cable T.V. The concept began in and has been actively pursued by the telecommunications industry through the CCITT.

Chapter 1 includes a brief technical development history of the telephone based telecommunications system to its current status, the evolution of ISDN from its conception to its present status, and the role of the central office. Topics covered include:

- The initial inefficient techniques using point-to-point pairs;
- The birth of a circuit switching central office with manual switchboards;
- The advent of automatic switches for the central office;
- The topology of the modern telephone network;
- Other types of telecommunication networks;
- The control of telecommunication networks;
- The role of the CCITT in the development of ISDN;

- Setbacks to the rapid realization of a global ISDN;
- And the development of ISDN products and services;

A formal description of ISDN standards and protocols and the role of the CCITT in their development is provided in Chapter 2. Also covered is a brief description of possible user applications and bandwidth requirements.

The initial effort of building an IBM XT PC based ISDN central office, one of a number ISDN research projects within the Computer Engineering Department at Iowa State University, is detailed in Chapter 3. Other ISDN projects include:

- A senior design team project of building an ISDN digital telephone with enchancements. The telephone is designed to interface to the central office at the U-Interface;
- A graduate student project of designing and building an ISDN B channel multiplexer. The device is to multiplex eight asynchronous lines into a single B channel;
- An independent senior design project of building an ISDN TA;
- A graduate student project of designing and building a high speed ISDN to Ethernet gateway;
- And a graduate level course that included writing the software required to implement ISDN protocols in the central office.

Chapter 4 covers the revision of the original central office design goals, the division of design responsibilities, and a description of the various hardware segments of the revised design. All segments except the U-Interface are covered in some detail.

Chapter 5 furnishes a description of the design of the U-Interface card. The additions to the original design are covered in detail, as well as an overview of the card's functionality. The Conclusion deals with the changes required to make the U-interface conform to recently passed standards, the existing state of the central office design, hardware testing procedures, results of the testing, and suggestions pertaining to the expandability of the design.

CHAPTER 1. THE EVOLUTION OF TELECOMMUNICATIONS

In the beginning were the words, "Mr. Watson, please come here. I want you." That was the initial spark leading to the current explosion in communications. The telecommunications industry has steadily evolved over the last 115 years, continuously changing due to technological advances and influx of customers.

Telephone Communications

Inventions Spawn Growth

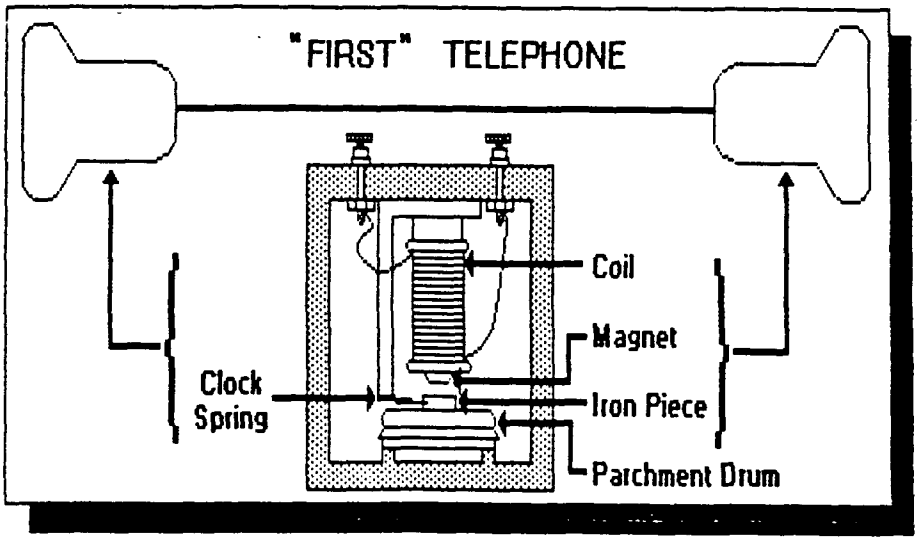


Figure 1.1: Alexander Graham Bell's Telephone

The Telephone Although a German scientist, Johann Philipp Reis, is believed to have invented the telephone, and a Chicago American, Elisha Gray, filed a patent the same day as Alexander Graham Bell, Mr. Bell has been historically recognized as the inventor of the device [28]. In January of 1876 in Boston, Massachussetts, the first telephone conversation took place between Mr. Bell, in the attic of his home, and his assistant Mr. Thomas Watson, on the ground floor. Immediately thereafter Mr. Bell sketched the design of his device, as in Figure 1.1, and applied for a patent, which was granted on his 29th birthday.

In 1877 Thomas Alva Edison of the USA invented the carbon microphone, as did Englishman Professor David Edward Hughes, who received the majority of credit for the invention in 1878. Therefore today's telephones contain a microphone transmitter and an electro-magnetic earphone receiver. Also in 1877 the first telephone service began as point-to-point pairs in Charleston, Massachussetts.

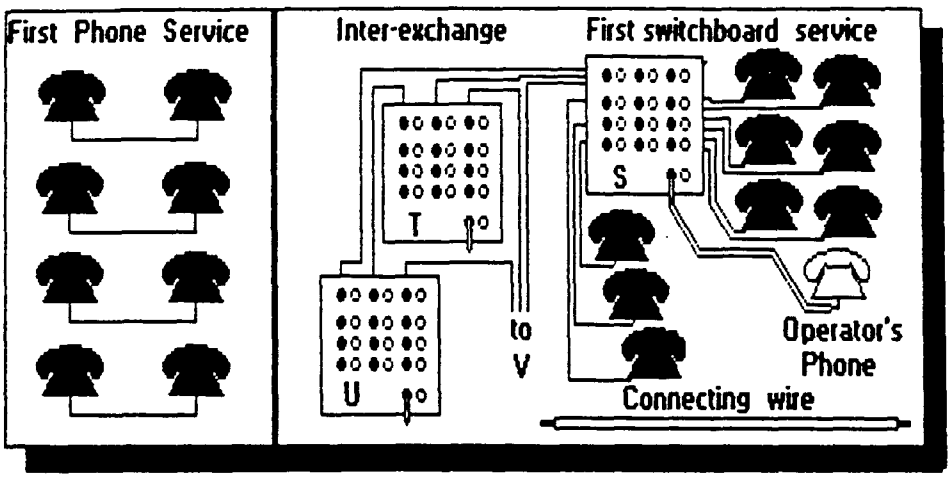


Figure 1.2: Early Service and Switchboard Service

Switchboards In 1878 a manually operated switchboard, the first telephone exchange and central office, was opened in New Haven, Connecticut, allowing eight subscribers to connect in pairs, as depicted in Figure 1.2. To respond to demand, larger switchboards were built and put in service. Coupled with intercity and trans-Atlantic coaxial cable distribution lines, switchboards allowed long distance point to point communication.

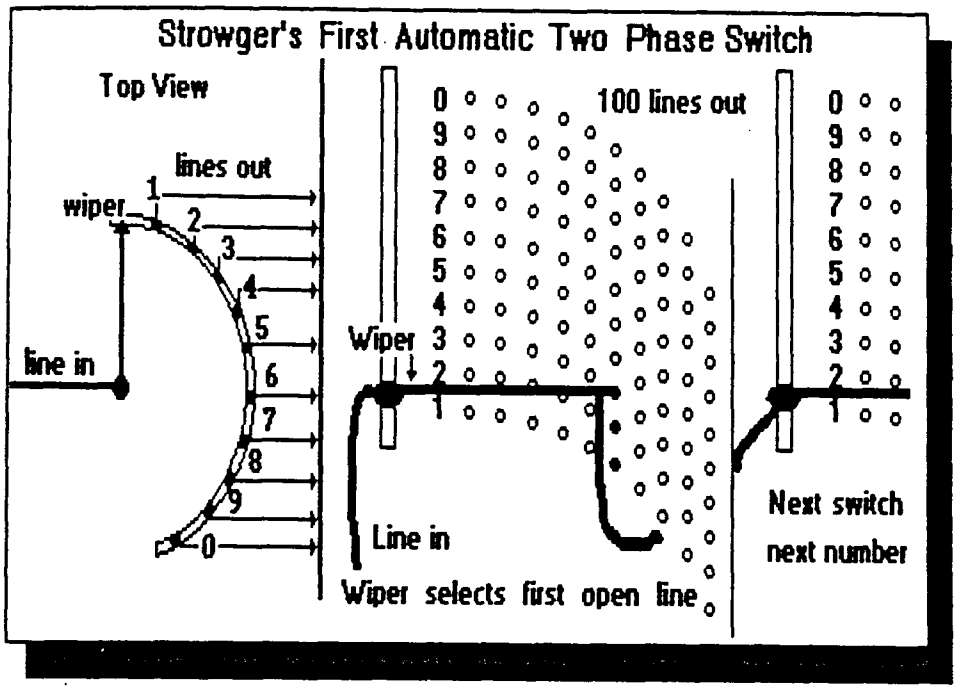


Figure 1.3: Automatic Two Phase Switches

Automatic Switches The automatic switch was invented by Mr. Almon B. Strowger in 1889, and allowed local direct dialing of other subscribers. The switch, illustrated in Figure 1.3, consisted of two parts for each number dialed, a column selector corresponding to the number dialed and a line selector which selected the first available, non-busy, line in the column of number dialed. Modern microprocessor

driven switches, using digital electronics and logic, are presently replacing the old electro-mechanical switches [24]. These new switches are implemented on a VLSI chip. They require less physical space and perform a wider variety of functions, such as buffering of information. They exhibit improved response time, without signal jitter due to the electro-mechanical switch bouncing [23].

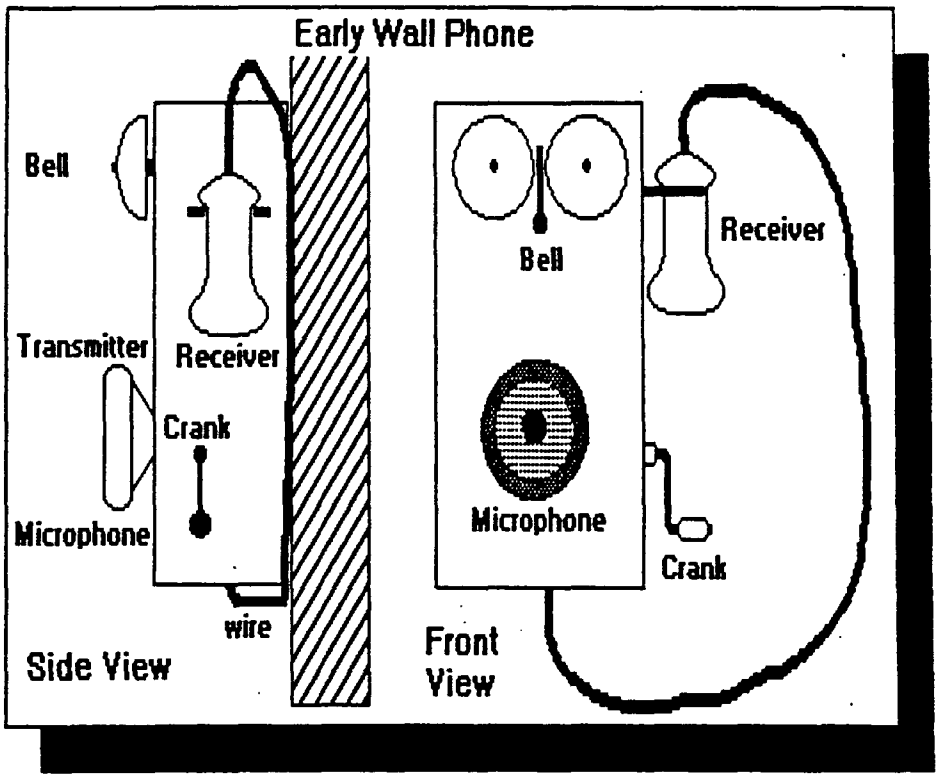


Figure 1.4: An Early Wall Phone

Subsequent Changes to Telephones In conjunction with electro-mechanical switches came telephones with dials. The dials replaced the crank generators, represented in Figure 1.4, used to call switchboard operators. Subscribers were assigned telephone numbers, so that a series of these switches could connect two subscibers,

using dial signals. Although the advent of automatic switches replaced the need for switchboard operators, switchboards remained in use in parts of the USA for local or long distance calls and in some businesses into the early 1970's [28].

Logic enhanced switches led to touch tone telephones, replacing the number dial used to generate signals for the switch wiper. However, touch tone telephones retained the use of analog based communication. The modern switches being placed in service have led to the development of digital based communication telephones. Although prior to the advent of these telephones, telephones used digital electronics to provide a wide variety of services, such as auto-redial, speed dialing, and message retention.

Modern Telecommunication Networks

Network Topology The typical topology of a telecommunications network, see Figure 1.5, consists of a backbone of central offices or switching centers, which are connected together, either directly, or indirectly through a tandem office via interoffice circuits. Each central office serves subscribers within a few kilometer radius. Several thousand subscribers may be connected to a single central office. Switches in various central offices must have the ability to communicate information to switches in distant central offices in order to perform efficient routing when establishing connections.

Equipment Not all telephone companies, worldwide, have modern equipment. Service varies not only between countries and companies, but within the geographical areas of the countries themselves. Third world countries and rural areas, where demand is small, may have used and antiquated equipment. Services offered in an

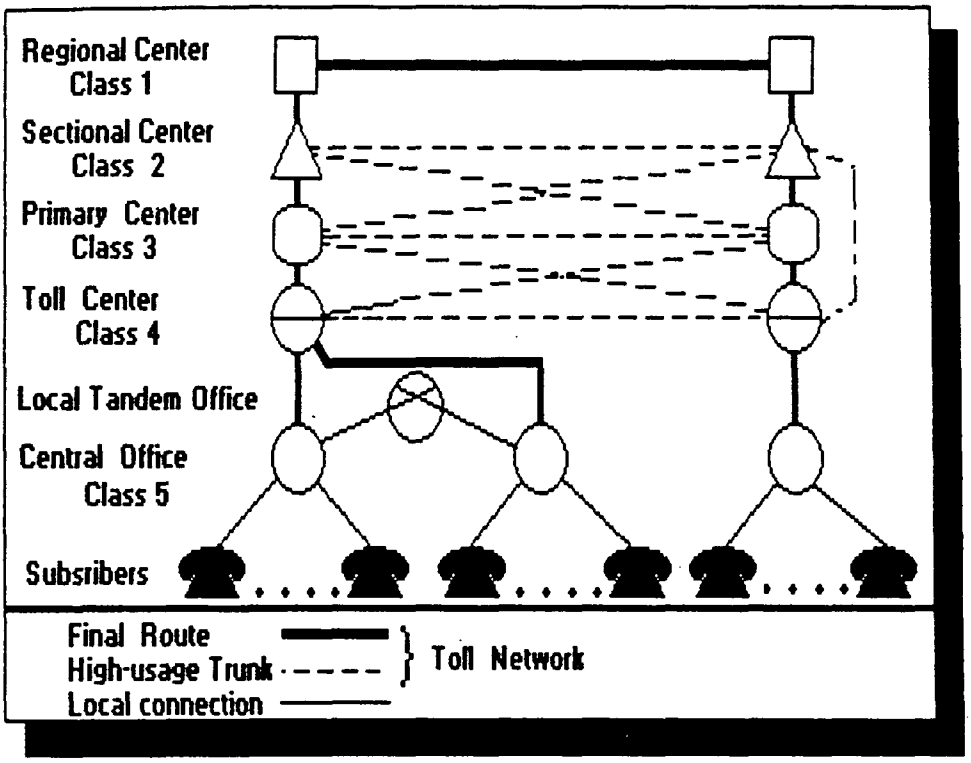


Figure 1.5: Telephone Network Switching Hierarchy

area are dependent upon the network equipment in that area.

Ownership and Control Most telephone companies outside of the USA are owned by the government, and virtually all are regulated by the governments of the countries in which they are located. In the USA early telecommunication companies were small, local, free enterprise entities. AT&T eventually monopolized the long distance distribution and most of the major local markets. The companies it didn't own, it could control indirectly because of its monopoly on the rest of the market.

Consequently, the FCC was created to regulate AT&T's activities and tariffs. Based upon an anti-trust lawsuit filed by the federal government in 1974, AT&T was forced to split its vast holdings in 1984. This resulted in the world's only free enterprise telecommunication's system, as well as a certain amount of chaos in the industry overall, since AT&T was the industry's leader[3].

Modern Free Enterprise System Although the splitting of AT&T and its 22 service subsidiaries theoretically brought reduced rates through competition, it also destroyed the previously uniform approach to introduce new technology and services. In order to compete as a long distance carrier and to realign its objectives and personnel, AT&T temporarily shelved some programs such as ISDN[3]. Standards enabling a uniform approach to a diversified problem were forsaken in lieu of profit in the new USA competitive marketplace.

The final results were:

- seemingly increased rates or no noticeable reduction for the consumer;
- seven large local distribution companies and several competing long distance

carriers;

- non-uniform implementation of a variety of new services;
- and the introduction of switches from various vendors that could not communicate outside of their own vendor's products.

Uniformity of equipment and enhanced service implementation became non-existent and consequently integration is more complicated.

Telecommunications

Definition of Telecommunication

The formal definition of telecommunications is the sending and receiving of messages over a distance by electrical methods [24]. Telephone networks are the most widespread, not only, in terms of geographic area and availability, but also, in terms of potential capacity and usage. But telecommunications does not only consist of telephone networks.

Other Forms of Telecommunication

Analog Entities The first telegraph was in service by 1839 in London, England. The wireless telegraph, which preceded public radio's inception in the 1920's, dates back to the 1890's. Public television became widespread in the United States after World War II, and satellite communication was introduced in the early 1960's [28]. Finally, access to coaxial cable television, Cable TV, became widespread during the late 1970's, and video teleconferencing facilities were available in the 1980's [24].

Computer Networks ARPANET, the first major computer network, originated in 1969 as a research network under the influence and control of ARPA, an agency of the U.S. Department of Defense. It used leased telephone lines to transfer information, data, between its original four nodes, geographical sites. By 1975 it had grown into an extensive network, and was put under the control of the Defense Communications Agency [4]. In 1974 IBM announced its development of SNA, the first distributed packet switched network, and made it commercially available [3].

Integration of Services

Evolution of the Concept

The Analog Environment In 1959 H. E. Vaughan proposed ISN, an integrated services network, which would bring most major telecommunication services into businesses and residences via public telephone lines [15]. The vast distribution network of the telephone industry, and the advances in and widespread use of automatic switches made this idea feasible. However the technology in 1959 was based upon analog signaling, and was, not only, unable to filter out noise between repeaters, but also, propagated noise end to end.

Digital Technological Advancements Digital multiplexing provided greater bandwidth utilization than analog FDM, as depicted in Figure 1.6 [14]. Advances in TDM, VLSI circuits using PCM for analog to digital and digital to analog conversion for digitized voice transmission, VLSI circuit implementation of smart switches, fiber optic transmission techniques and cables, and digital noise filtering techniques at repeaters made fully integrated services more feasible. The inherent delay and echo

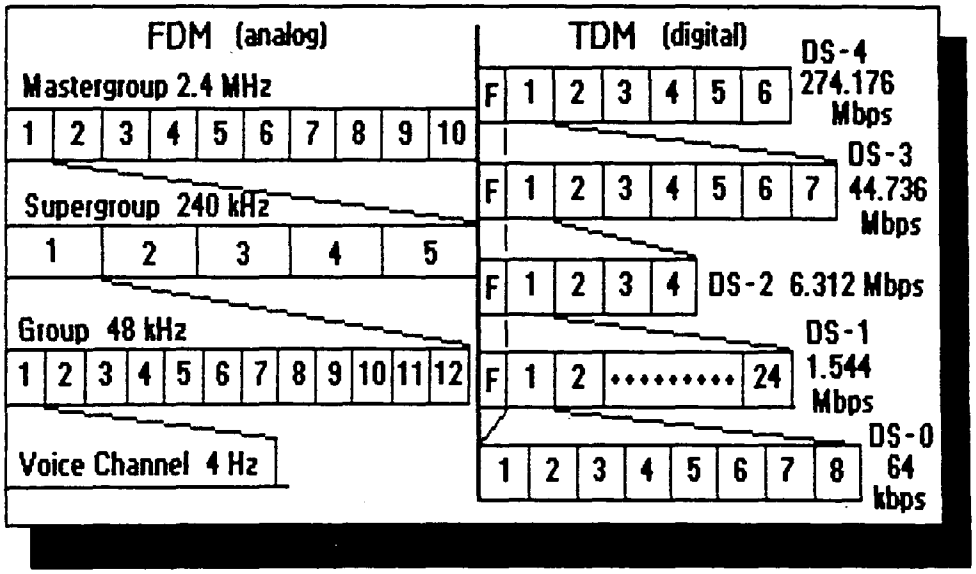


Figure 1.6: U.S. Telecommunication Multiplexing Hierarchies

Table 1.1: CCITT Study Groups

NUMBER	TITLE
I	Definition, operation and quality of service aspects of telegraph, data transmission and telematic services
II	Operation of telephone network and ISDN
III	General tariff principles including accounting
IV	Transmission maintenance of international lines, circuits and chains of circuits; maintenance of automatic and semi-automatic networks
V	Protection against dangers and disturbances of electromagnetic origin
VI	Outside plant
VII	Data communications networks
VIII	Terminal equipment for telematic services
IX	Telegraph networks and terminal equipment
X	Languages and methods for telecommunications applications
XI	ISDN and telephone network switching and signaling
XII	Transmission performance of telephone networks and terminals
XV	Transmission systems
XVII	Data transmission over the telephone network
XVIII	Digital networks including ISDN

problems of digitized voice transmission became history.

CCITT Preference Is Digital In 1971 during a meeting of the CCITT's Study Group XI, assigned to study and to recommend standards for switching and signaling, shown in Table 1.1, the term ISDN was first introduced. Despite the fact that disputes continued until 1988 over whether an integrated service should be implemented in analog, digital, or a combination of the two, the CCITT pushed the ISDN concept, founding Study Group XVIII in the late 1970's specifically for the purposes of setting goals and studying standard proposals for ISDN [15].

The Evolution of ISDN

CCITT's Standards

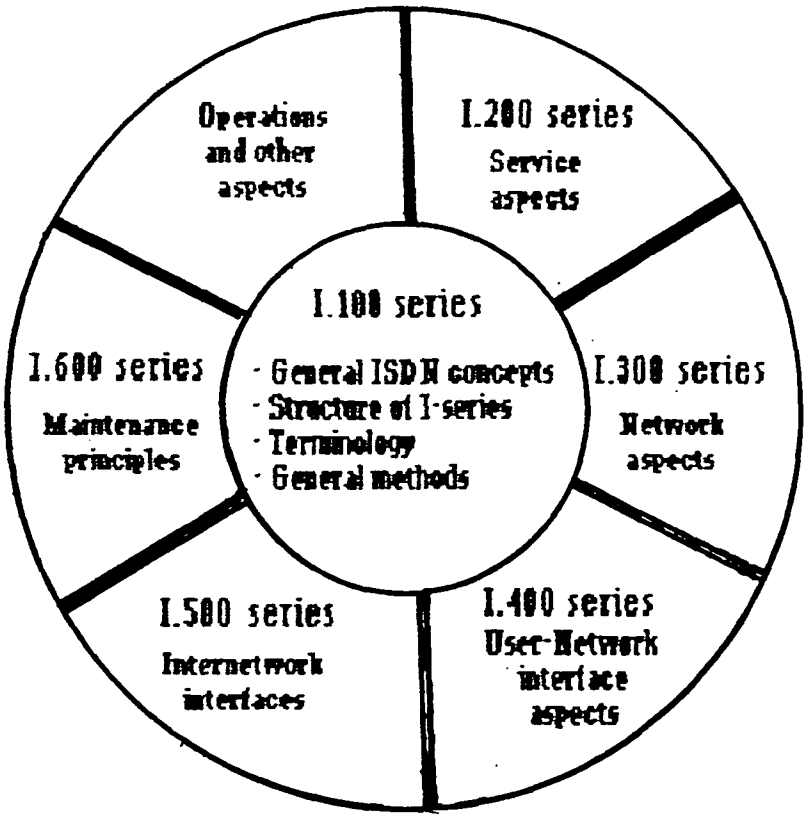


Figure 1.7: CCITT's Recommendations

From 1980 to 1984 the I-series standards were partially developed and published. By 1984 the CCITT had the majority of its study groups involved in developing standards for ISDN, and with the influx of fiber cable into major distribution lines directed focus on the development of B-ISDN standards. More standards were adopted in 1988, with 2B1Q the most recent [16].

Major Setback

However the industry's leader, AT&T, which initially had been totally committed to ISDN, was derailed temporarily by the consequent upheaval of reorganization of the company due to Judge Green's decision in 1982 to split the company. This as previously outlined, not only led to a delay in implementation in the United States, but also slowed the research and standards process. Many of ISDN's services were implemented by providers outside of the singular approach of the CCITT's ISDN standards [2].

Evolution of Products and Services

The first time-division digital switch was developed by Western Electric, an AT&T subsidiary, in 1976, and ISDN digital phones appeared in the 1980's. Part of AT&T's 800 service is implemented in ISDN, and a renewed effort is being made due to potential business LAN and WAN applications and high rate data transfer from remote PC's. Also the DOD has expressed an interest in the ISDN backbone concept.

Furthermore fiber optics based B-ISDN, in the research stage, has the potential of offering a wider variety of services to a wider range of subscribers due to the high bandwidth capabilities of fiber cable. Some applications and their bandwidth requirements are outlined in Figure 1.8 [1]. Layer-2 and Layer-3 standards are similar to ISDN's, however due to vast differences in Layer-1 mediums, B-ISDN standards in this layer use different multiplexing and transmission techniques. SONET with a rate of 155.52 Mbps and ATM have been adopted as standards [7].

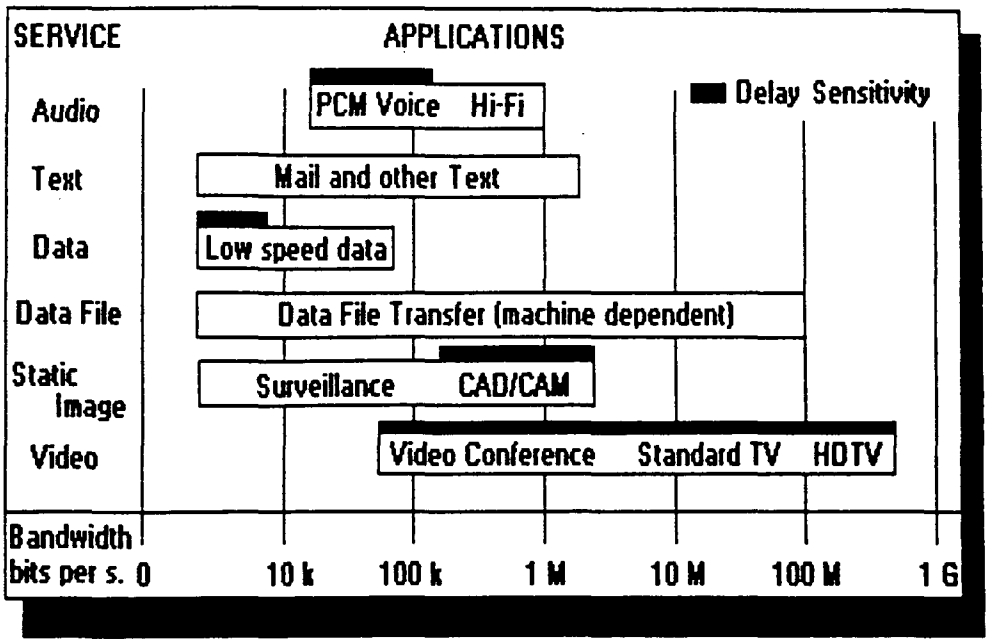


Figure 1.8: Application Bandwidth Requirements

CHAPTER 2. ISDN

Services

ISDN is an evolving technology designed to provide a set of common user interfaces to a wide range of telecommunication and networking services on both a local and a global basis via telephone distribution systems. Some of the user services that ISDN is expected to provide are outlined in Table 2.1 [14].

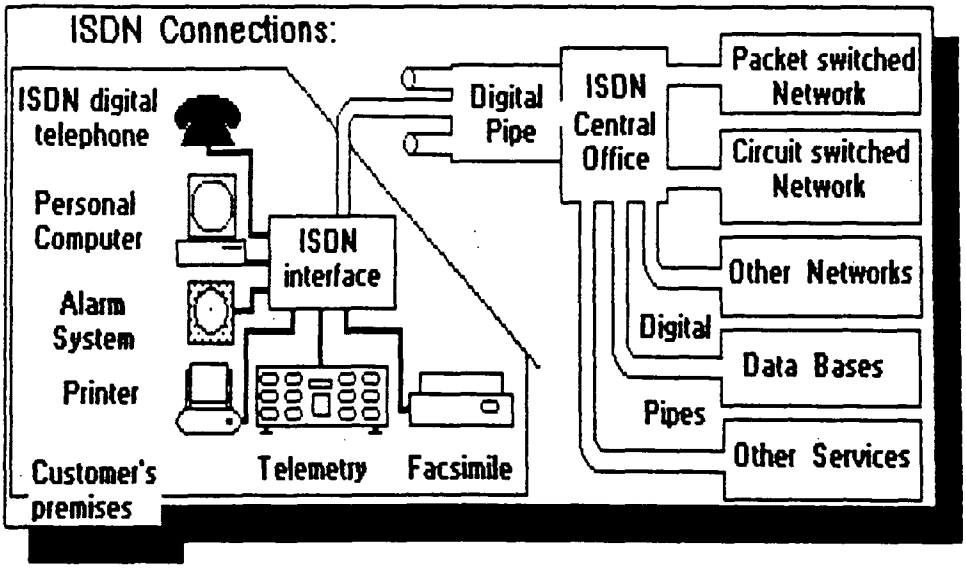


Figure 2.1: Conceptual View of ISDN Services to User-Interface

User to services interfaces are conceptually represented in Figure 2.1. ISDN services are available to the user only through the user's central office. Central offices

Table 2.1: Possible ISDN Services and User Applications

ISDN SERVICE	APPLICATIONS
Circuit Switched Services	Basic telephone service Call screening via caller's number recognition call tracing Selective call forwarding Junk facsimile recognition (deny advertizing access) Elelectronic funds transfer Video transactions Video telephones Nuisance (also runaway or kidnapped children) Automatic call waiting
Packet Switched Services	Elelectronic mail enhancements Conference calls Video teleconferencing Telemetry (911) Automatic call distribution based on caller's number
Networking Services	PBX networks (LANs) LAN interconnections Public network access Automatic voice response to database access Database caller authorization Remote high speed data transfer Programmed education
Other Services	Automatic call return Selective (personalized) messages Extension of business services into homes Automatic dial telemarketing (until response) Automatic caller data retrieval (previous communication history) Security systems

in the United States are in the process of conversion to offer ISDN services, however 200 ISDN subscribers are necessary to make conversion cost effective. Charges are about double that of normal telephone service, but the cost of on premise equipment appears to be the primary prohibitive factor. A minimal cost of equipment with network termination would run in excess of two thousand dollars.

Functional Architecture

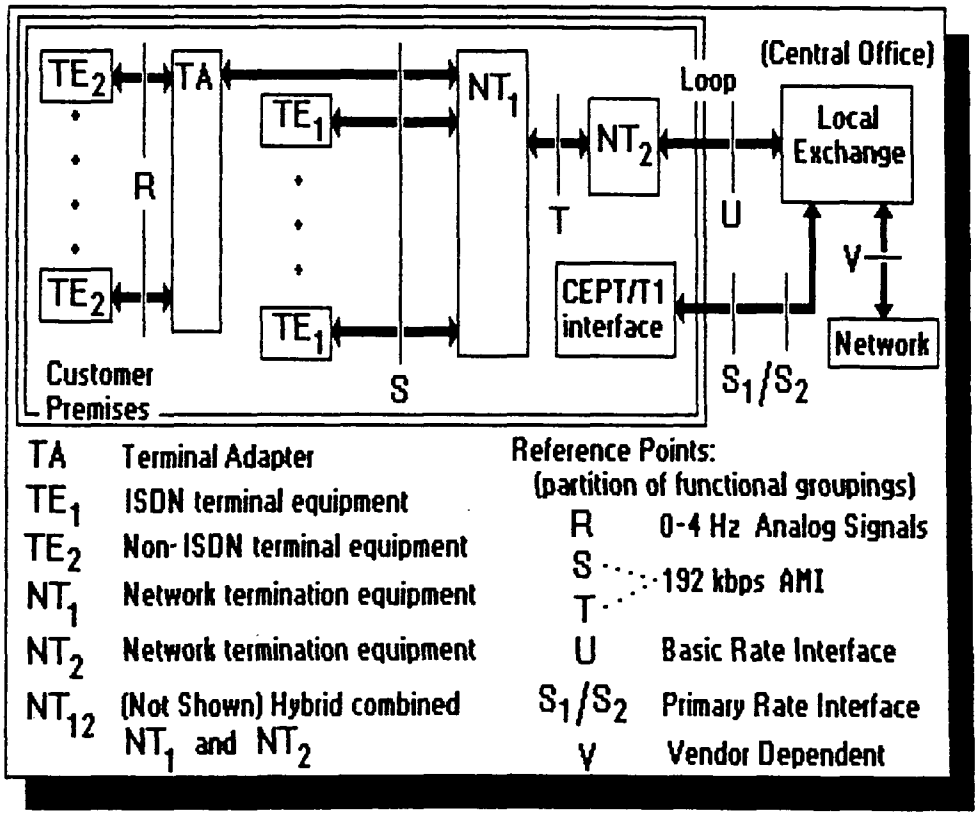


Figure 2.2: ISDN User-Interfaces

An ISDN topology depicting both equipment and interfaces, reference points, is illustrated in Figure 2.2. Reference point designations date back to the advent

of switchboards, see Figure 1.2. The exact definition of the interface between the customer's premises and the central office, however, is not clearly defined, due to the scope of implementation on the customer's premises [16].

European and North American (including Japan) standards differ in the network termination points at the customer's premises. In Europe NT1 terminates the network. NT2 functions are performed at the central office via the T-Interface. The North American customer's installation includes the NT2, so that the central office supports the U-Interface. The ISU central office supports both the S/T-Interface, a combination of the S-Interface and the T-Interface, and the U-Interface.

Equipment, depicted in Figure 2.2, is defined as follows:

1. TE1. A customer premise device supporting the ISDN S-Interface.

2. TE2. A customer premise device not supporting the ISDN S-Interface.

3. TA. A device supporting the ISDN S-Interface between TE2 equipment and ISDN's NT1.

4. NT1. Customer premises network termination equipment supporting the Physical Layer protocols as outlined in Figure 2.3.

5. NT2. Network termination equipment supporting the Data Link and some Network Layer protocols as outlined in Figure 2.3.

The NT2 could stand alone as a PBX or be combined with an NT1 to form a hybrid NT12, network termination device, supporting the S/T-Interface. The interfaces depicted in Figure 2.2 are defined as follows:

1. R – Twisted pair with analog voice signal, 0-4 hz rate.

2. S – Two twisted pairs with ISDN digital bitstream, 192 kbps rate.

3. T – Two twisted pairs with ISDN digital bitstream, 192 kbps rate.

4. U – Twisted pair with ISDN 2B1Q bitstream, 160 kbps, 80 baud rate.

5. S1/S2 – T1 or fiber optic cable with PRI rate of 2.048 or 1.544 Mbps.

6. V – Optional and vendor dependent.

Standards

CCITT I-Series Recommendations

The CCITT's goal is that the set of ISDN standards and protocols being developed will eventually be the standards and protocols of all wire based telephone distribution systems worldwide. The goal for fiber based distribution systems is the total adoption of B-ISDN standards and protocols. Far in the future, fiber will replace twisted pairs and ISDN will be phased out in lieu of B-ISDN, but there is no immediate danger of that due to the cost of converting all existing twisted pairs to fiber optic cable.

ISDN standards are to be implemented in both on premises subscriber's ISDN equipment and the various telephone systems' offices' equipment. The CCITT's evolving, I-series Recommendations as of 1990 are outlined in detail in Appendix A. The I-series recommendations are quite extensive, covering not only all technical aspects of ISDN, but also committee procedures and service rates.

ISDN Reference Model

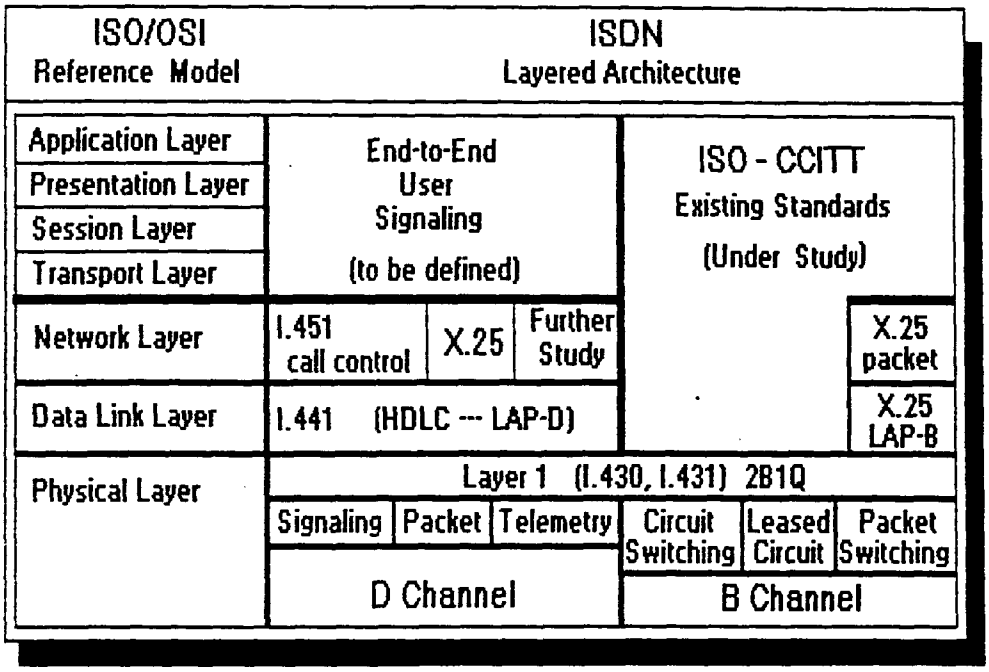


Figure 2.3: ISDN Reference Model

Link-to-Link Layers The ISDN reference model best depicts the technical standards and protocols of interest. The ISDN reference model is based upon the bottom three layers of the OSI/ISO reference model, and is depicted in Figure 2.3. There are two basic reasons for this. The CCITT, the largest proponent of ISDN, is concerned primarily with the implementation aspects of standards and protocols in telephone networks. This translates to the bottom layers of the OSI/ISO model.

As depicted in Figure 2.4, services are provided to a layer by the layer directly below it via SAPs. Primitives are used in the communication between the layers to identify the service requested or the response. Data, information, and options are passed as parameters to the primitives. Headers are added at each of the lower four

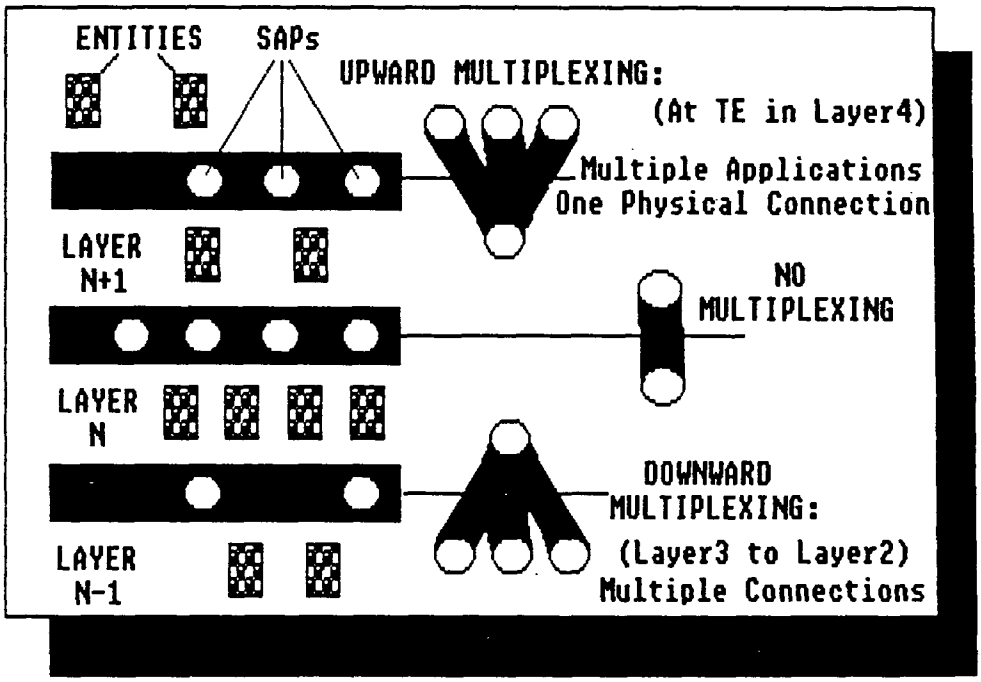


Figure 2.4: ISO/OSI Model Interlayer Communication

layers to the data.

End-to-End Layers The Application Layer through the Transport Layer of the OSI/ISO model are end-to-end layers, and define the protocols required for the exchange of information between same layer entities on two communicating host machines. Protocols for these layers will be developed as businesses become interested in implementing ISDN LANs and WANs. As yet, a complete set of standards has not been developed for these layers by the ISO in the OSI reference model.

The Physical Layer

Specified Functions

As illustrated in Figure 2.3, I.430 (BRI) and I.431 (PRI) specify the Physical Layer standards. The functions specified in these user-network interface standards are [14][16]:

- Activation and deactivation of the physical circuit, reducing power consumption when the channels are idle.
- Contention resolution on the D channel for point to multipoint configurations.
- Encoding of digital transmission via AMI at the S/T interface and 2B1Q at the U-Interface.
- Faulty terminal identification and isolation, via loopback testing.
- Full duplex transmission of B and D channels.
- Multiplexing of channels to obtain BRI and PRI transmission requirements.

- Power feeding from the NT, source, to the TE, sink.
- Terminal identification.

Transmission Rates

Table 2.2: ISDN Channel Types

CHANNEL	PURPOSE	BIT RATE
B	Bearer Services	64 kbps
D or D_{16}	Signaling and Packet Mode	16 kbps (BRI)
D_{64}	Data	64 kbps (PRI)
H_0	Six B channels	384
H_1	All Available H_0 Channels	
	H_{11} (24B)	1536 kbps
	H_{12} (30B)	1920 kbps
H_2	Proposed B-ISDN	
	H_{21}	32.768 Mbps
	H_{22}	43-45 Mbps
H_4	Proposed B-ISDN	132-138 Mbps

At the Physical Layer in the model, ISDN's transmission medium consists of local digital signaling over twisted pair wires and long-haul multiplexed digital signaling over T1 carriers or fiber cables where available. Due to the influx of fiber distribution lines and fiber based LANs, B-ISDN standards are being developed. ISDN standards specify three basic channel types as detailed in Table 2.2. Interoffice signaling, CCIS, is out-of-band at the rate of 800 bps on a separate network [16].

User-Interface Rates

Basic Rate Interface Combinations of B and D channels compose two user interfaces, BRI and PRI. Conceptually to the user, these can be thought of as digital

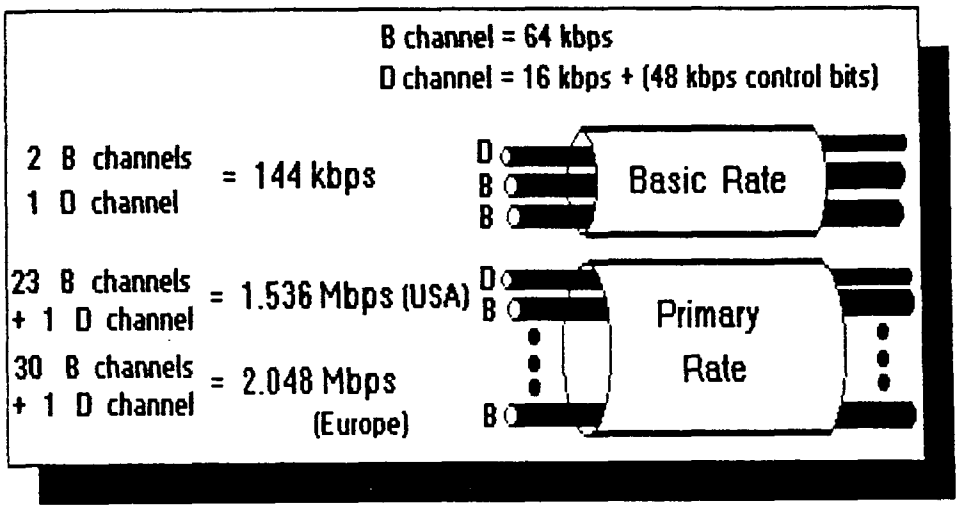


Figure 2.5: ISDN User-Interface Transmission Rates

pipes as depicted in Figure 2.5. The basic rate channel's effective rate is 144 kbps, with 48 kbps used for overhead, control and contention resolution at the S and/or T interfaces on the customer's premises, as detailed in Figure 2.2. B channels are used for voice and data, while the D channel is used for data, such as a virtual terminal, and for signaling, such as control of the B channels [14].

Primary Rate Interface Unlike the basic rate interface, which is standard worldwide, the primary rate interface is defined by two standards. The North American primary rate channel uses 8 kbps as framing or synchronization bits, one every 193 bits. The D_{64} channel is used for data and control. The European primary rate looses 64 kbps in overhead, leaving a maximum effective data transfer rate of 1.984 Mbps less framing. The North American maximum effective data transfer rate is 1.536 Mbps less framing [16].

Reference Point Signaling Standards

ISDN standards stipulate different signaling techniques at the U and S/T reference points, as depicted in Figure 2.2. Not only are the rates different but so are the voltages and techniques. The U reference point signals each designate two bits, while the S and T reference points only one. Also the interleaving of D and B channels is different.

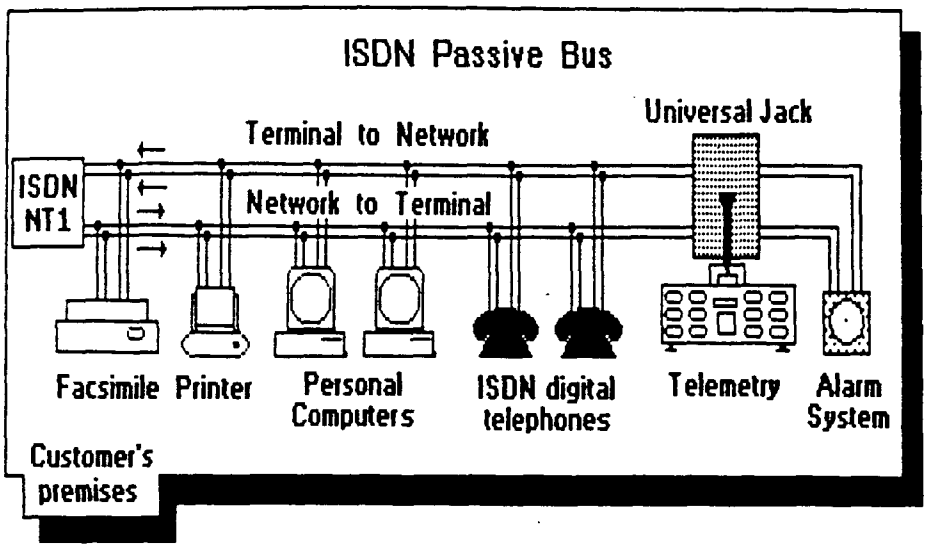


Figure 2.6: ISDN Multi-point, Passive Bus Configuration

S/T-Interface Signaling Standard The bitstream at the S and T reference points, as illustrated in Figure 2.7, supports the BRI of 144 kbps plus control and overhead for a total rate of 192 kbps. A single NT can support up to eight TEs. These can be configured as point-to-point, TE to NT, or point-to-multipoint, such as a passive bus, diagrammed in Figure 2.6.

E bits echo the incoming D channel bits and are used to resolve contention for the D channel between competing TEs. The TEs monitor the E bits and after waiting

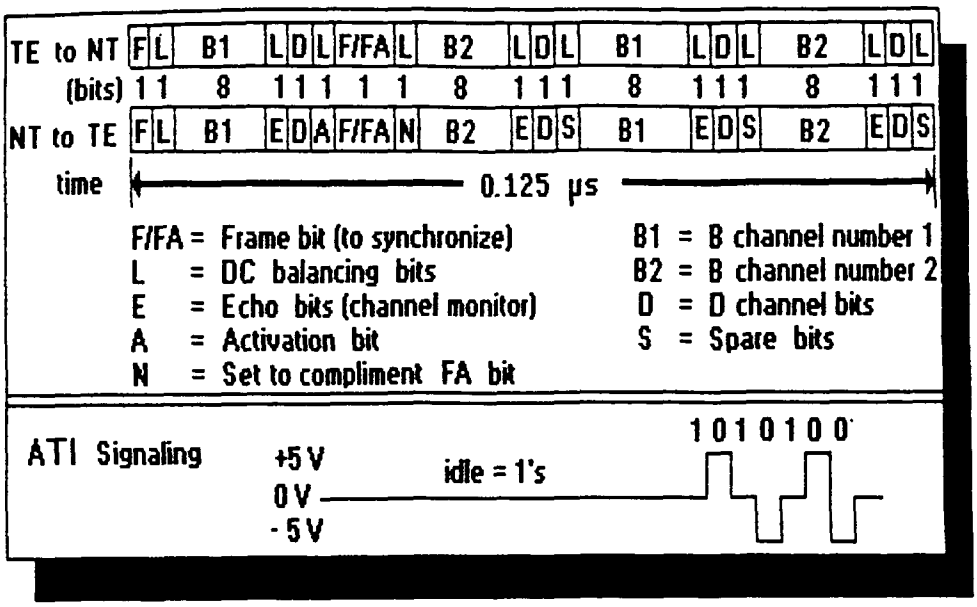


Figure 2.7: ISDN S/T-Interface Bitstream Format

for either 8, 9, 10, or 11 successive logical 1's, depending upon a TE's priority and the type of information it has to transmit, the TE transmits a logic 0 to request the channel. If a conflict occurs, the TE must backoff and renew the waiting process. Priority is based upon which TE last used the channel and is used to prevent starvation, as depicted in Table 2.3.

Table 2.3: D-Channel Contention Priority Assignment

PRIORITY	This TE Last Used the Channel	WAIT PERIOD
Data/Signal	No	8
	Yes	9
Telemetry	No	10
	Yes	11

Logic 1 transmits at 0 V to conserve power when the channels are idle. Logic 0 transmissions alternate between positive and negative voltages, and therefore con-

flicts are easily detected. Pseudo-tenary signaling, also referred to as alternate zero inversion, AZI, is specified in the standards and is illustrated in Figure 2.7 [16].

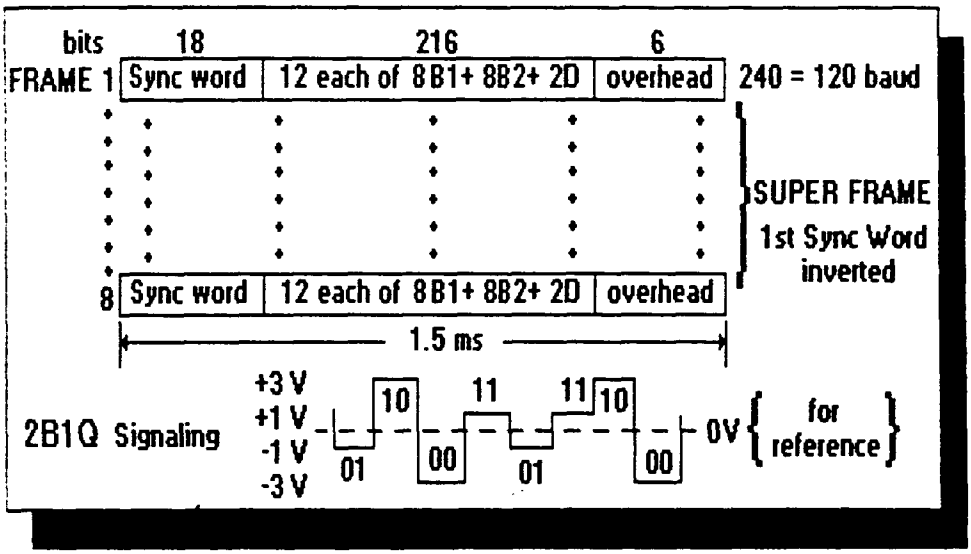


Figure 2.8: ISDN U-Interface Bitstream Format

2B1Q: U-Interface Signaling Standard The U reference point bit rate is 160 kbps, with two bits represented in each signal, as illustrated in Figure 2.8. Therefore the signal rate is 80 kbaud. While this is far less than the S/T bit rate of 192 kbps, it is still adequate to carry the basic rate of 144 kbps. While the S/T bitstream B and D channel interleaving is 8 B1, 1D, 8 B2, 1D, the U bitstream interleaving is 8 B1, 8 B2, 2D.

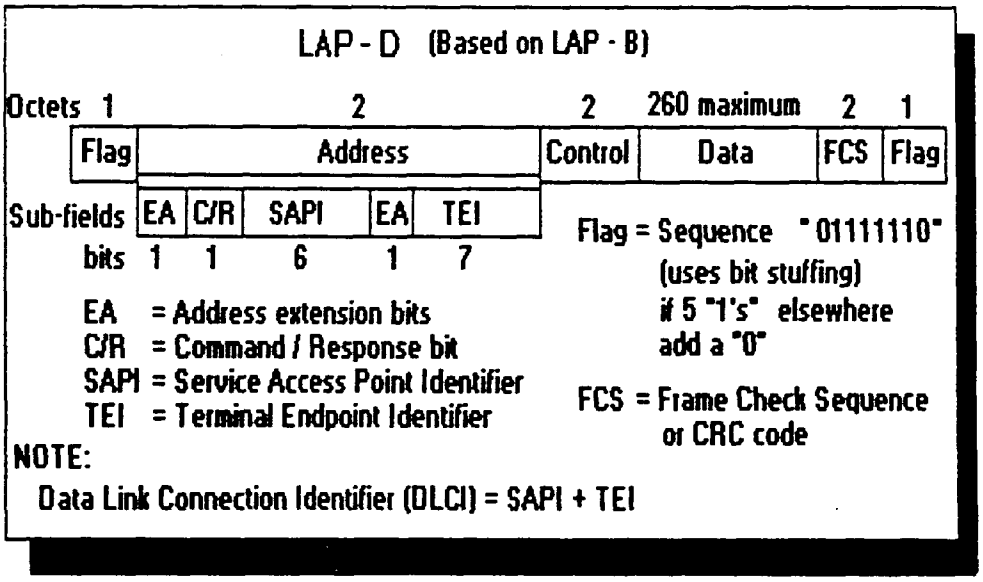
The Data Link Layer

As illustrated in Figure 2.3, I.441 LAP-D and X.25 LAP-B are standards approved for the D and B channels respectively in the Data Link Layer, Layer 2 of the

CCITT Recommendations. The D channel supports control signaling, packet switching, and telemetry via LAP-D. The B channel supports circuit switching, leased circuits, and packet switching via LAP-B. The B in LAP-B does not denote the B channel but signifies balanced signaling. LAP-B is a subset of HDLC, and LAP-D is based upon LAP-B, as referenced in Figures 2.10 and 2.9 [8].

LAP-D: The D Channel Interface

Figure 2.9: LAP-D Frame Format



Frame Format The LAP-D frame format is illustrated in Figure 2.9, above. The flags are used for frame synchronization, due to the variable length data field and the ability to extend destination addresses of both the SAP and the TE. The EA bit is set from '0' to '1' to extend these address fields, the SAPI and the TEI, which combined form the total data link destination address. The FCS field performs error detection. Bad packets are discarded, as are packets when only a singular flag is

detected in the bitstream. To avoid this happening naturally in the address, control, data, and FCS fields, bitstuffing is used as outlined in the figure.

Functions The primary functions of the LAP-D, I.441, protocols are as follows:

- Establish, maintain, and terminate Data Link connections for both channels.
- Handle multiplexing at the customer's premises, between TEs and within a single TE running multiple applications, or a single application requiring multiple simultaneous traffic types.
- Provide error detection as previously defined.

LAP-B: The B Channel Interface

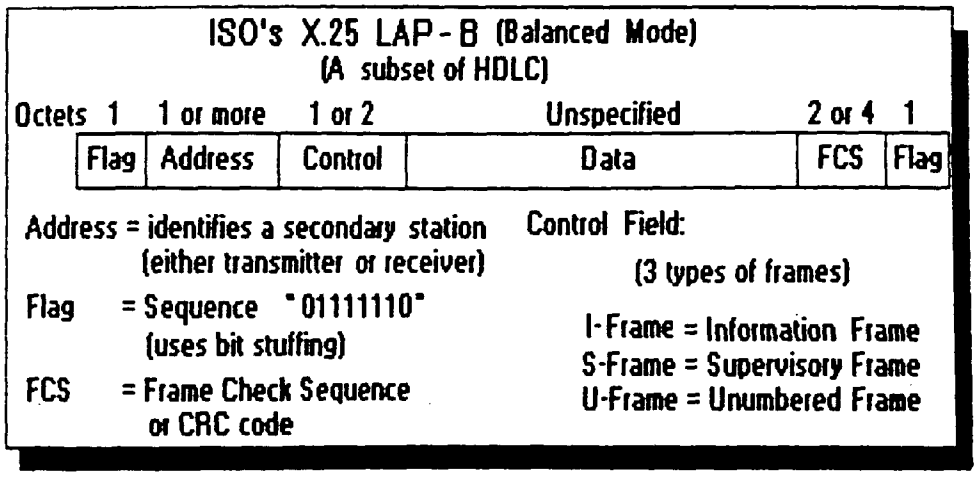


Figure 2.10: LAP-B Frame Format

The LAP-B frame is outlined in Figure 2.10. Like LAP-D, bit stuffing is used to keep the synchronization flags unique. Error detection is also provided in the FCS

field using the CCITT defined polynomial [19]:

$$G(x) = x^{16} + x^{12} + x^5 + 1.$$

The definition of the control field frame types are as follows [8]:

- I-Frame contains normal data and information.
- S-Frame contains control information, such as acknowledgements.
- U-Frame contains options and network management information.

Packetized data is exchanged over the B channel, whether the connection is circuit switched, leased, or packet switched. X.25 levels 2 and 3 are used to establish a virtual circuit and exchange packets.

The Network Layer

The accepted standards for Layer 3, as outlined in Figure 2.3, are I.451, or Q.931, and ISO's X.25. The functions performed at the Network Layer are [12]:

(a) The processing of primitives for communicating with the Data Link Layer.

(b) The generation and interpretation of Layer 3 messages for peer-level communication.

(c) The administration of timers and logical entities (e.g. call references) used in the call control procedures.

(d) The administration of access resources including B channels and packet-layer logical channels (e.g. Recommendations X.25).

(e) Checking to ensure that services provided are consistent with user requirements.

General functions that may also be performed are:

(a) Routing and relaying.

(b) Network connection control.

(c) Conveyance of user-to-network and network-to-user information.

(d) Network connection multiplexing.

(e) Segmenting and Reassembly.

(f) Error detection.

(g) Error recovery.

(h) Sequencing.

(i) Congestion control and user data flow control.

(j) Restart.

The ISU central office is designed to support all specified standards except 2B1Q at the U-Interface. The initial design uses a pseudo U-Interface, as the project was started prior to the acceptance of the standard. At a later date, LAP-D and Q.931 is to be implemented in software as another Master of Science thesis project.

CHAPTER 3. THE ORIGINAL CENTRAL OFFICE DESIGN

Geetha Venkataraman, a Computer Engineering Master of Science graduate in 1990, completed a partial design and hardware implementation of the original central office as part of her graduation requirements. Her thesis was based upon that partial design.

Availability of accurate and detailed information on the original ISU central office design from the designer was sparse. The thesis was difficult to follow, and only inaccurate hand sketched schematics were available. Consequently the major sources of information used to evaluate the design were the MITEL "Microelectronics Data Book", the hardware implementation circuitry, parts of her thesis, Dr. Douglas W. Jacobson, her major professor, and Angela Bradley, a Computer Engineering graduate student assigned to the design of the S/T-Interface.

Goals

The principle design goals of the original ISDN central office project at ISU were:

1. To implement current CCITT ISDN local exchange standards (e.g. central office) in an IBM XT PC providing:

   (a) Layer 1 and partial Layer 2 functions in readily available hardware;

(b) a primary rate interface for the user;

(c) a basic rate U-Interface for the user;

(d) a basic rate S/T-Interface for the user;

(e) routing from user to user via a digital switch;

(f) and timing signal generation as required.

2. Software running on the IBM XT PC, providing the following functions:

(a) implementation of the X.25 and Q.931 protocols;

(b) and perform all routing through the digital switch,

3. The user physical access through special ISDN telephone jacks.

4. Minimal complexity in the implementation of the central office design.

The PC Card

A partial design was implemented on a single PC board, as illustrated in Figure 3.1, using MITEL's ST-BUS family of ISDN system components. The hardware design consisted of six distinct functional groupings, namely:

1. The ST serial bus, with a bandwidth capacity meeting basic rate, North American primary rate, and European primary rate requirements.

2. The PC bus interface, consisting primarily of bus drivers.

3. Timing circuitry to provide the timing required on the ST bus.

4. U-Interface MITEL ISDN chips and supporting circuitry consisting of:

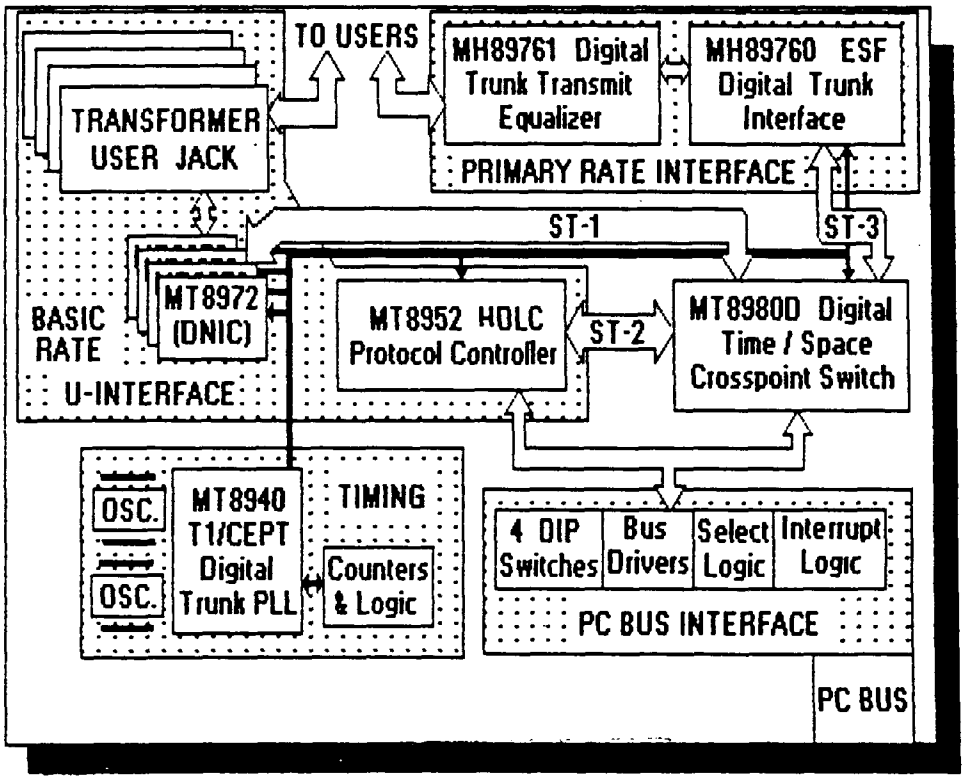


Figure 3.1: The Original ISU Central Office Hardware Design

(a) four Digital Network Interface Chips (DNICs);

(b) four 2:1 transformers with capacitors and resistors, providing the user a physical interface to the line pins on the DNICs;

(c) an HDLC Protocol controller, providing X.25 level-2 functions, data buffering, and address recognition for routing.

5. Primary rate interface to a T1 line using a Digital Trunk Interface chip and a Digital Trunk Transmit Equalizer.

6. A Digital Crosspoint Switch providing routing over 16 ST busses which consist of 256 incoming channels and 256 outgoing channels.

The MITEL ST-BUS

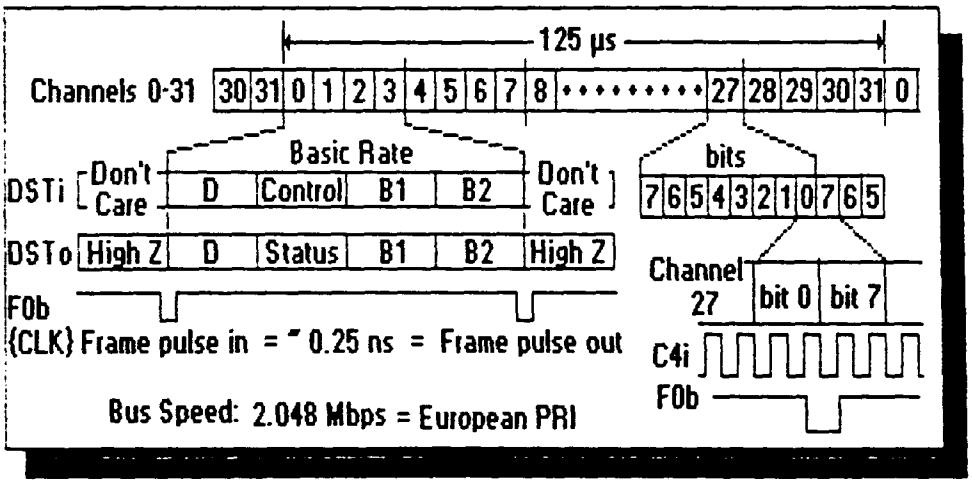


Figure 3.2: The ST-BUS BRI Channels and Timing

Complying with the ISDN standards and PCM requirements of eight thousand voice samplings per second, the ST-BUS is based upon the overall time frame of 125

microseconds, as depicted in Figure 3.2. The ST-BUS is serial and uni- directional, and therefore two busses are required for full duplex transmission capabilities as required in ISDN. Each bus is time divided into 32 channels, which are subdivided into 8 bit segments within each sampling period.

There are two types of busses defined, data and control, each requiring two directional busses: input, from the user to the network; and output, from the network to the user. The control buses were not used in this design. Data bus pins and busses are denoted as DSTi or Di for input and DSTo or Do for output. When used at the Basic Rate Interface, each bus can support multiplexing of up to eight interfaces, which in turn support multiplexing of TEs over the B and D channels [19].

As illustrated in Figure 3.2, each BRI device is alotted four channels, the B and D channels plus a STi control channel or a STo status channel. The control and status channels are used to communicate with the interface chips, especially at the U-Interface. Due to the different interfaces supported (BRI and PRI), the time subdivision of the busses, and the multiplexing ability of the bus, several clock speeds are required for synchronization.

ST-BUS Timing Generation

ST-BUS Waveforms The primary chip used to generate timing for the ST-BUS system is the MT8940. In the original central office design, four signals were required, as depicted in Figure 3.3. The MT89760 Digital Trunk Interface required the $\overline{C2i}$ and the $\overline{F0i}$ framing pulse. The $\overline{C2i}$ synchronizes bit transmission, just as the $\overline{C4i}$ signal in all the other MITEL circuits used in the design. All circuits require the frame pulse to synchronize the four channel segments on the ST-BUS.

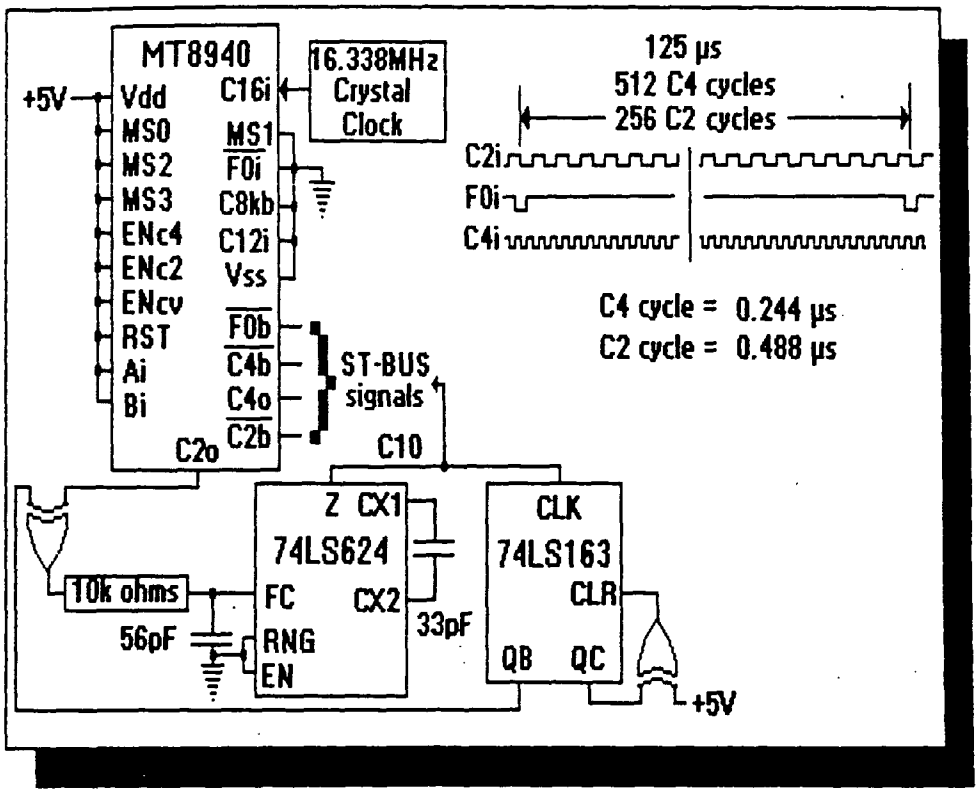


Figure 3.3: The ST-BUS Clock Signal Generation Diagram

The C10 signal, produced by the synchronous timing generation circuit, is used by the MT8972B DNICs at pin number 16. The synchronous timing generation circuit is composed of two exclusive-or gates, two capacitors, one resistor, a 4-bit synchronous counter, 74LS163, and a voltage controlled oscillator, 74LS624.

The PC Bus Interface

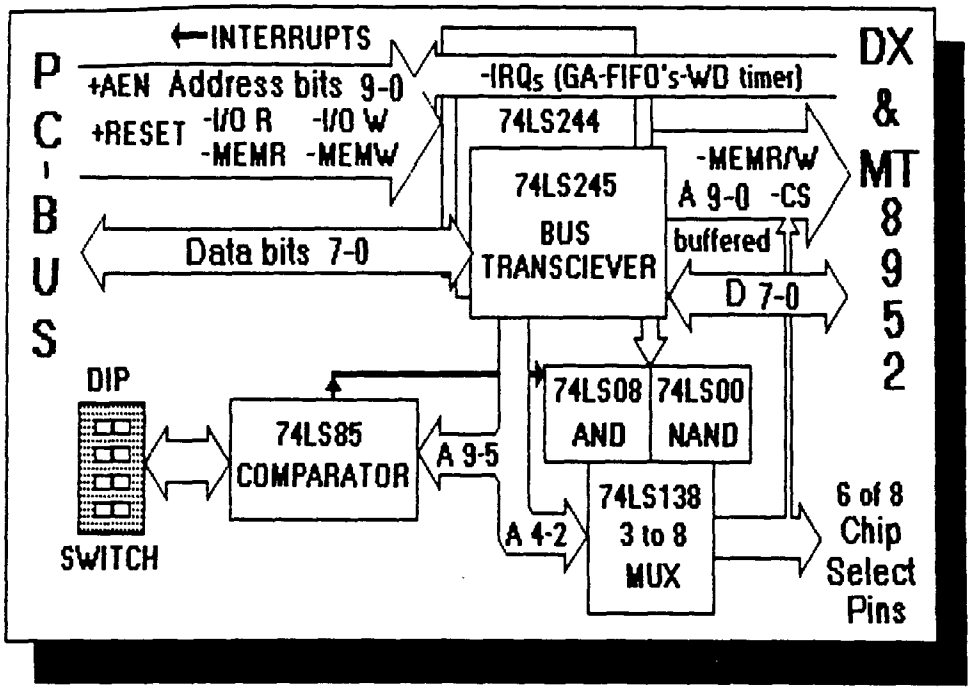


Figure 3.4: PC-Bus Interface Block Diagram

The PC bus interface on the card on which the original central office was built was prewired via printed circuits. It consisted of the devices diagrammed in Figure 3.4, and offered 10 buffered address lines 8 buffered data lines, buffered I/O Read and Write, reset, 8 chip selects, and interrupt logic.

The Primary Rate Interface

The PRI was incomplete due to a missing trunk line interface chip. Therefore since it is inactive, little detail on the PRI of the design is included. The primary piece of hardware in the design of the PRI is the MT89760, ESF Digital Trunk Interface, which possesses the following features [19]:

- With a T1 Digital Trunk Transmit Equalizer, MT89761, a complete interface to a bidirectional T1 link.
- D3/D4 or ESF framing and SLC96 compatible.
- Two frame elastic buffer with 32 microsecond jitter buffer.
- Insertion and detection of A, B, C, and D status bits.
- Signaling freeze and optional debounce.
- Robbed bit signaling, overall or per channel.
- Frame and superframe synchronization signals.
- AMI encoding and decoding.
- Overall, per channel, and remote loop around.
- Eight kiloHertz synchronization output.
- Digital phase detector between T1 and ST-BUS.
- Bipolar violation count, frame error count, and CRC error detection.

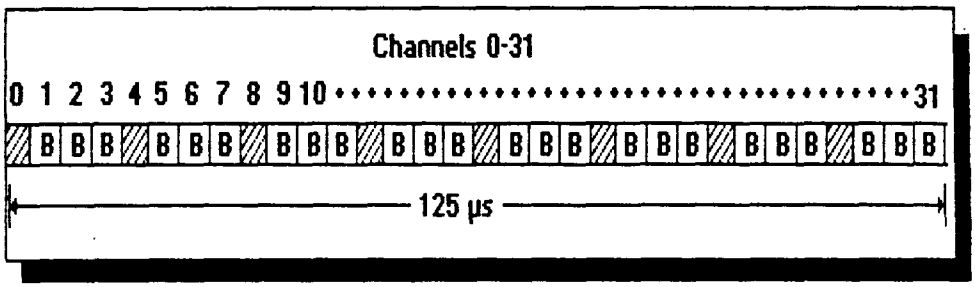


Figure 3.5: ST-BUS Channels at the PRI

The MT89760 interfaces directly to a Digital Crosspoint Switch via the ST-BUS. The channel allocation on the ST-BUS for the PRI differs from the channel allocation for the BRI, as illustrated in Figure 3.5, above. Additional timing signals are also required for digital ST-BUS bit insertion and T1 line synchronization, as illustrated in Figure 3.5. Function control and status can be monitored through registers, via a serial control ST-BUS at the switch by the PC. Timing is provided by the MT8940, as previously depicted in Figure 3.5.

The MT8980D Digital Crosspoint Switch

DX's Features and Functions The MT8980D, DX, is the key device in the original design. All communication on the serial busses must pass through it, and a communication path exists to the PC. The primary functions and features of the DX are [19]:

- MITEL ST-BUS compatible, with 8 line by 32 channel inputs and 8 line by 32 channel outputs forming a 256 port non blocking switch.
- Low power consumption (30mW) and +5 Volt single power supply.
- Microprocessor-control interface, provides access to individual channels.

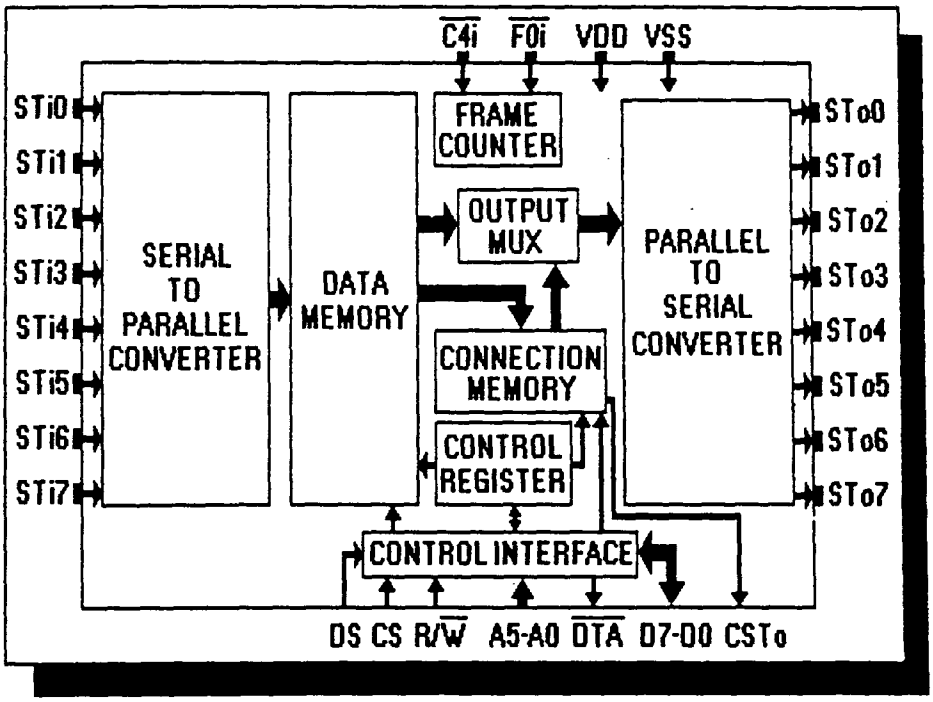


Figure 3.6: The MT8980D Functional Block Diagram

- Three-state capabilities on all eight serial outputs.

The MT8980D and MT8981D are the two digital switches offered by MITEL. The MT8981D supports four input ST busses and four output ST busses. The MT8980D supports eight busses of each, as illustrated in Figure 3.6, resulting in a switching capacity of 256 channels input by 256 channels output. For this design the MT8981D would be sufficient, but for expandability the MT8980D was chosen. The MT8980D is cascaded in designs requiring more than 256 channels.

Memory Description The MT8980 contains two distinct memories, the data memory and the connection memory. The data memory consists of 256 eight bit words, corresponding to the 256 eight bit incoming channels. The connection memory also consists of 256 locations, corresponding to the 256 eight bit outgoing channels, with each location consisting of low and high parts of eight bits each. The high order bits are channel control bits, while the low order bits designate the address of the input channel's data stored in data memory, as illustrated in Table 3.1.

Access by the PC or microprocessor is accomplished directly via normal data, control, and address bus to memory interface connections. The data memory is a read only memory, while the connection memory is a random access memory and is accessible only through the control register.

The Control Register Data in the Control Register consists of mode control, memory select, and stream address bits, as depicted in Table 3.2. Bit 7 allows split memory operations as indicated. Message mode allows the PC or microprocessor to write or broadcast to all channels on all output busses simultaneously, via each

Table 3.1: MT8980D Connection Memory Bits

BIT	NAME	DESCRIPTION
		HIGH PART
7-3	Unused	read as logical '0's
2	Message Channel	When '0' low order bits address data memory When '1' the low order bits are outputted
1	CSTo bit	Value of this bit to CSTo pin one channel early
0	Output Enable	When ODE pin is high and Control Register bit 6 is '0', the output driver is enabled thereby allowing the construction of switching matrices
		LOW PART
7-5	Bus Addr.	Address the incoming bus 0-8 ('100' is STi4)
4-0	Channel Address	Address the incoming channel 0-31 bit 4 is the most significant bit

Table 3.2: MT8980D Control Register Bits

BIT	NAME	DESCRIPTION
7	Split Memory	'1' reads from data and writes to low connection memory '0' memory select bits determine subsequent operations
6	Message Mode	'1' & ODE pin '1', low connection memory is put on bus '0' connection memory bits determine channel output
5	Unused	
4-3	Memory Select Bits	'00' Not to be used '01' Data memory is read only '10' Connection memory - low part '11' Connection memory - high part
2-0	Stream Address Bits	The binary number expressed refers to the input or output ST-BUS stream corresponding to the subsection of memory made accessible for subsequent operations

connection memory location's low order bits. Otherwise when bit 6 is 0, the high order connection word dictates output.

The memory select bits designate which of the three memories can be read from or written to. Stream address bits together with the pins A4-0, determine the address of the memory location being accessed. A5 asserted low provides access to the Control Register, which can be read from as well as written to.

The control bits must be changed prior to changing reading or writing modes. The ODE pin, when low, can cause all outputs to go to high-impedance, therefore it is wired high. High-impedance is therefore achieved only via software control.

Functional Description Serial data is received at each of the eight bus inputs, converted to eight bit parallel words and stored in the 8x256 data memory, which can be read by the PC or microprocessor to ascertain destination addresses for switch routing. Switching is accomplished by writing to the low connection memory locations, after control register setup. Any input channel can be switched to any output channel. All ST-BUS frame and bit timing is derived from the $\overline{F0i}$ and $\overline{C4i}$ pins.

The U-Interface Components

The DX pulled double duty, because it aided in implementing the U-Interface. It allowed the PC access to the DNICs' control registers via the C-channels. One set of busses (e.g. input and output) connected the switch to a group of 4 daisy-chained MT8972B Digital Network Interface Circuits, while a second set of busses connected to a MT8952 HDLC Protocol Controller, which performed X.25, Level-2 functions.

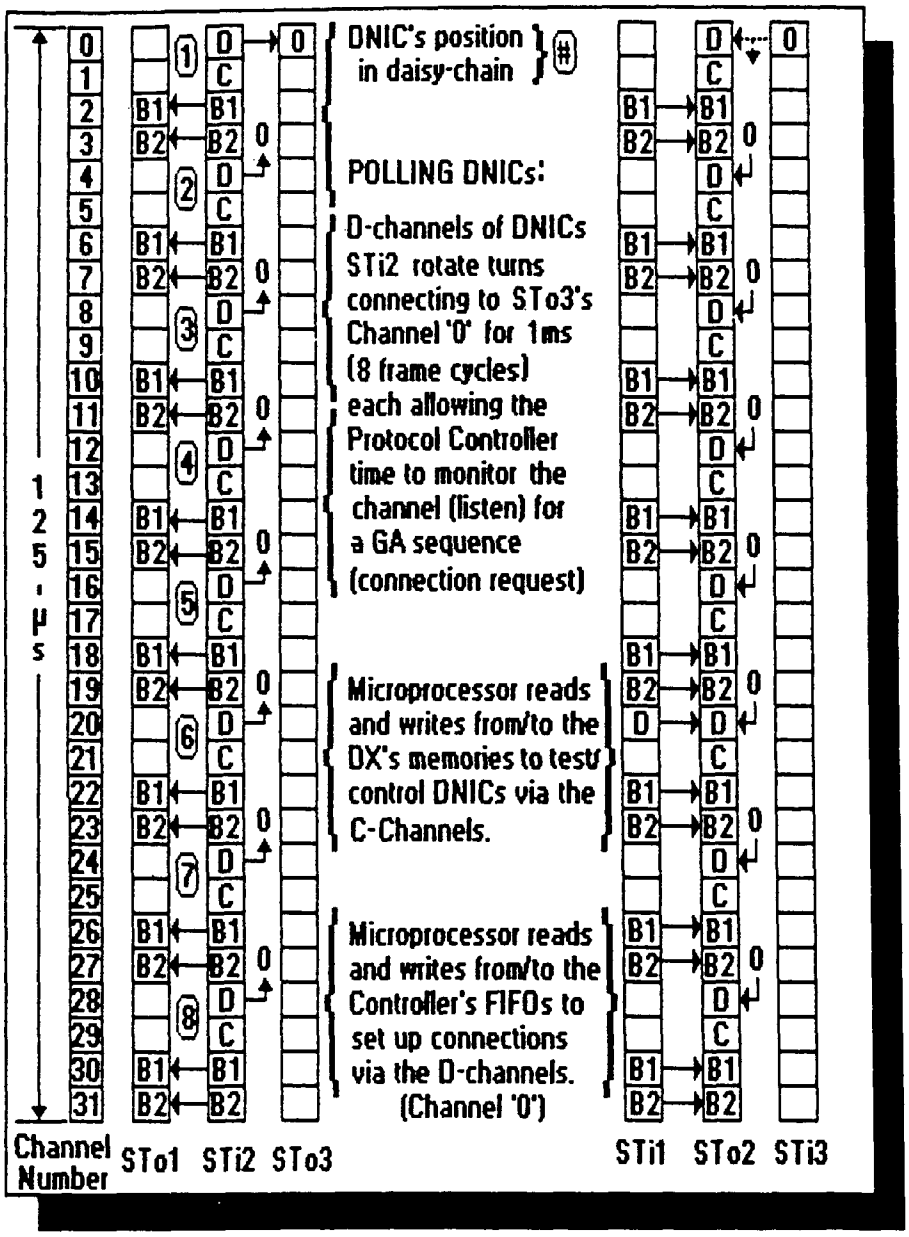


Figure 3.7: C-Channel DNIC Control Routing

The DX switched the incoming C-channels from the DNIC bus to the outgoing bus of the Protocol Controller, establishing a control path to the DNICs. The DX could also communicate directly with the DNICs via low connection memory and data memory, as in Figure 3.7. Each DNIC's B channel was also switched to channel 0 going to the Controller in a predefined order. The Controller monitored the channel and when a GA sequence was detected sent an interrupt to the PC.

MITEL's MT8972B Digital Network Interface Circuit

DNIC Features and Functions The MT8972B, DNIC, was designed primarily as a U-Interface device for ISDN, but may be used in other applications such as a high speed, short distance modem. Some of the DNIC's functions and features allowing such diversity are [19]:

- Full duplex transmission over a single twisted pair.
- Selectable 80 kbps or 160 kbps line rate.
- Adaptive echo cancellation.
- Maximum line range of 4 km at 160 kbps or 5 km at 80 kbps.
- ISDN compatible 2B+D data format.
- Transparent modem compatibility.
- ST-BUS compatible.
- Low power consumption of 50mW.
- Single 5 Volt power supply.

Additional functional flexibility is provided within the ISDN environment, and consequently the DNIC offers several modes of operation, which are illustrated in Table 3.3. The DNIC converts line signals to ST-BUS format, and vice versa, to provide a common interface for networking to other ISDN components. Full duplex interface to the user is accomplished via a 2:1 transformer and a twisted pair. Line signaling was implemented using biphase signaling instead of 2B1Q as defined in ISDN U-reference point standards.

Table 3.3: MT8972B Mode Definitions

MODE	FUNCTION
SLV	SLAVE: timing extracted from line data and is output to the system
MAS	MASTER: timing supplied by system clocks (ST-BUS timing)
DUAL	DUAL PORT: Control and D channel are active on one bus, B channels are active on another
SINGL	SINGLE PORT: Control, B and D channels are active on same bus
MOD	MODEM: non formatted line data is handled by the DV port at 80 or 160 kbps
DN	DIGITAL NETWORK: data configured according to ISDN standards
D-C	D BEFORE C-CHANNEL: D-channel is transmitted before C-channel
C-D	C BEFORE D-CHANNEL: C-channel is transmitted before D-channel
ODE	OUTPUT DATA ENABLE: high impedance during power up

Modes of Operation Mode 0 was chosen in order to daisy-chain DNIC's, providing multiple interfaces with a minimal amount of supporting hardware. It provides DN, ODE, SINGL, MAS, and D-C operating modes. In DN (Digital Network) mode the line carries the ISDN data format, including a housekeeping bit on the control (C) channel. Single port mode allows access to the control, B and D channels on the same ST-BUS, as in Figure 3.2. ODE allows serial port outputs to be tristated to prevent damage on power up. MAS (Master) mode allows the DNIC to operate

via external ST-BUS timing.

Biphase Line Signaling The DNIC deviates from the latest adopted CCITT U-Interface signaling standard, 2B1Q, by using biphase line signaling, shown in Figure 3.8. A 2B1Q coding example was described in Chapter 2. When the DNIC was designed, 2B1Q was still being researched. Biphase signaling was a proven, cost effective technique that was readily available on the market. Performance is the primary advantage of 2B1Q, expanding the effective distance of transmission by over 25%. Cost, two twisted pair lines instead of one as in biphase signaling, and signal recovery complexity are the primary disadvantages.

2B1Q requires six to eight times more bit history to cancel out signal echo than does biphase signaling. The primary reason for this is that 2B1Q produces a bandwidth four times narrower than biphase. This reduces noise interference, but since pulses output on the line tend to develop long tails, it also leads to intersymbol interference between consecutive pulses. Cleaning up this interference leads to the more complex circuitry required for 2B1Q.

Table 3.4: MT8972B Status Register

BIT	NAME	FUNCTION
0	SYNC	Synchronization: when '1' indicates Lin sync is acquired
1-2	CHQual	Channel Quality: the farther from 0 the better the SNR
3	Rx HK	This is the received housekeeping from the other end
4-7	DNIB	Reserved for future functionality

Internal Registers The C-channel is used for communication between the DNIC and the system. This is accomplished by writing to and receiving from the

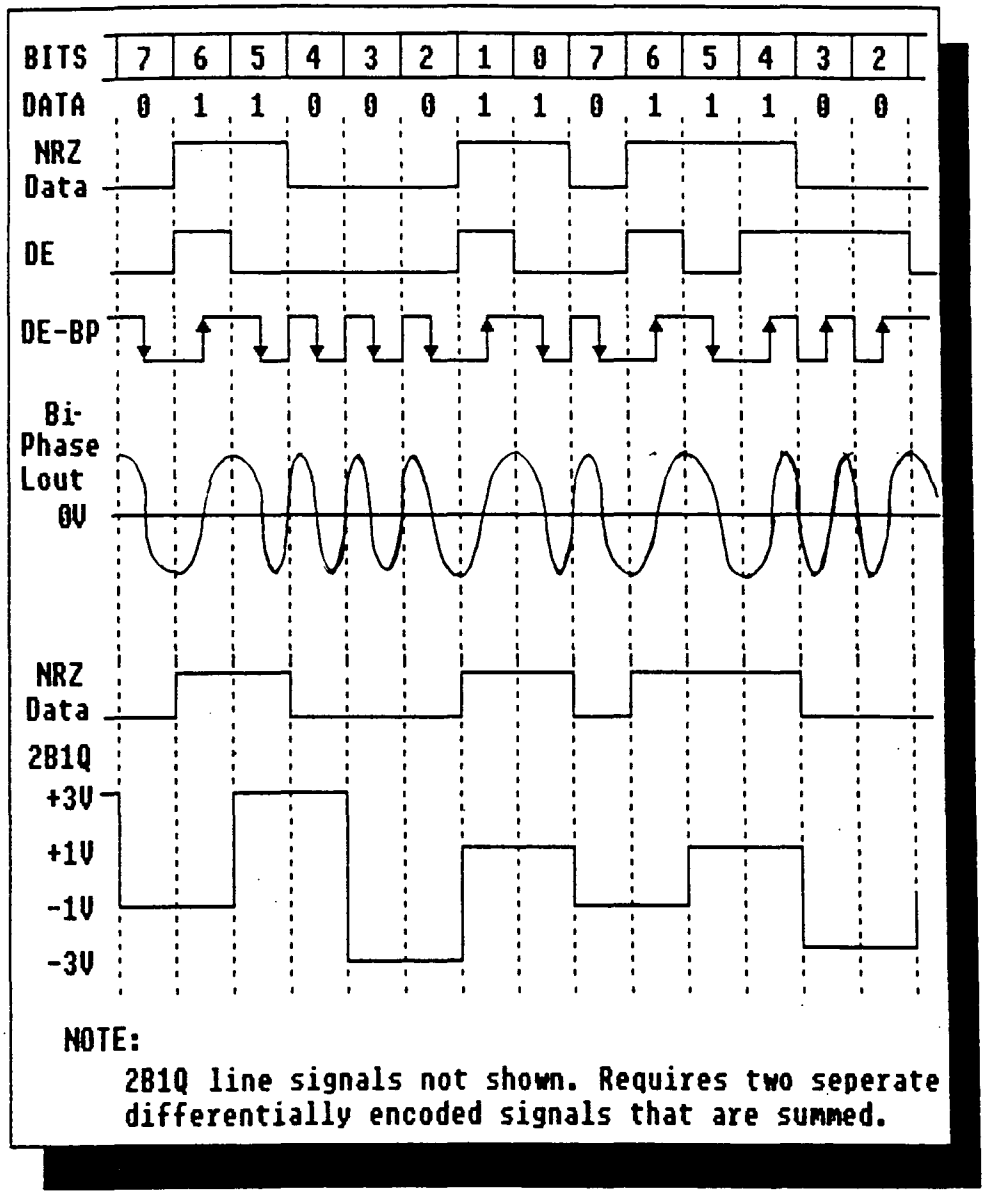


Figure 3.8: Line Signaling Waveforms

DNIC's internal registers. The DNIC contains three registers defined as follows:

- the control register, is a write only register whose functions are detailed in Table 3.5;
- the diagnostic register, is a write only register whose functions are detailed in Table 3.6;
- and the status register, is a read only register whose functions are detailed in Table 3.4;

Table 3.5: MT8972B Control Register

BIT	NAME	DESCRIPTION
0-1	Reg Sel	Register select: must be '00' to select control register
2	Future	must be set to '0'
3	BRS	Bit Rate Select: '0' is 80 kbps, '1' is 160kbps
4	DNIB	D-channel in B slot: active when '1'
5	PSEN	Prescrambler/Deprescrambler Enable: active when '1'
6	ATTACK	Set to '1' on power up for fast echo canceller convergence
7	TxHK	Transmit housekeeping bit: '1' active, '0' inactive

The Control Register is used to establish bit rates when used as a modem, control the transmission of the housekeeping bit on the Lout line, and control some onboard functions. All of the registers are accessed via the C-Channel through the Protocol Controller by the PC.

The Diagnostic Register is used for testing of the lines, the ST-BUS, and the DNIC's internal functions. Testing is performed both at power up and during normal operations via the housekeeping bit. Results of some of the testing procedures are stored in the Status Register, which also monitors channel quality. Other results are

Table 3.6: MT8972B Diagnostic Register

BIT	NAME	DESCRIPTION
0-1	Reg Sel	Register select: must be '01' to select diagnostic register
2-3	Loopback	'0 0' testing functions disabled – normal operation '0 1' DSTi internally looped back to DSTo for system testing '1 0' Lout internally looped back to Lin for system testing '1 1' DSTo internally looped back to DSTi for end-to-end test
4	FUN	Force UNsync: active when '1' to test synchronization
5	PSWAP	Polynomial Swap: active when '1' swaps scrambling and descrambling polynomials
6	DLO	Disable Line Out: active when '1' sets Lout to bias voltage
7	Unused	Must be set to '0' for normal operation

extracted directly from the bus at the MT8980. Using the DX for testing allows normal polling operations in the Protocol Controller, such that while one DNIC is tested another DNIC is monitored.

The HDLC Protocol Controller: MT8952

Features and Applications The MT8952 HDLC Protocol Controller is the pivotal device in the U-Interface design. The functions and features that center around it are [19]:

- Formats data as per CCITT's X.25 Layer-2 standards.
- Go-Ahead sequence (interrupt) generation and detection.
- Directly accessible registers for flexible operation and control via PC or microprocessor parallel port.
- Nineteen byte FIFOs in send and receive paths, digital serial busses.

- Handshake signals for multiplexing data links.
- High speed serially clocked output at 2500 kbps.
- ST-BUS compatible with programmable channel selection and separate timeslot for control information.
- Independent watchdog timer.
- Facility to disable protocol functions.
- Low power ISO-CMOS technology.

The wide variety of functions and the ability to control them, combined with the variety of distinctly unique configurations and applications in an ISDN environment, enables the MT8952 HDLC Protocol Controller to be used in several applications. The primary applications in which the MT8952 can be used are [19]:

- Data link controllers and protocol generators.
- Digital sets (e.g. terminal equipment), PBX's, and private packet networks.
- D-channel controller for ISDN basic access.
- C-channel controller to DNICs.
- Interprocessor communication.

Internal Functions The Protocol Controller's functional blocks, as depicted in Figure 3.9, can be grouped as follows:

- parallel port, used as the interface to a microprocessor and the MT8952;

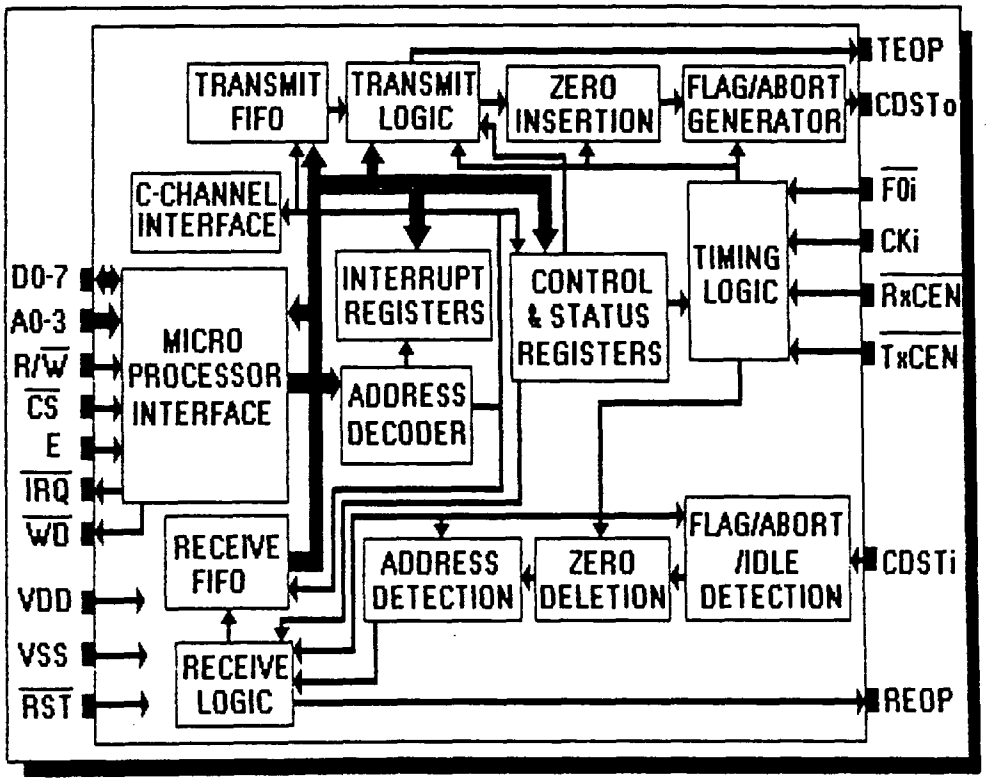


Figure 3.9: The MT8952 Functional Block Diagram

- transmit section, used to buffer, manipulate, and transmit data serially;
- receive section, used to buffer, manipulate, and receive data serially;
- control and status registers, used to direct the Protocol Controller's operation.
- and the parallel-serial interface, used to monitor and initiate data, primarily for DNIC communication.

Table 3.7: MT8952 Register Addresses

ADDR BITS	REGISTERS	REGISTERS
A3-A0	READ (high) PIN	WRITE(low) PIN
'0 0 0 0'	FIFO status	
'0 0 0 1'	Receive Data	Transmit Data
'0 0 1 0'	Control	Control
'0 0 1 1'	Receive Address	Receive Address
'0 1 0 0'	C-Channel Control (Transmit)	C-Channel Control (Receive)
'0 1 0 1'	Timing Control	Timing Control
'0 1 1 0'	Interrupt Flag	Watchdog Timer
'0 1 1 1'	Interrupt Enable	Interrupt Enable
'1 0 0 0'	General Status	
'1 0 0 1'	C-Channel Status (Receive)	

Registers The ability to control the functionality of the HDLC chip depends solely upon accessing the eleven registers on board. Access is accomplished via the PC or microprocessor's busses four lowest address lines, A3-A0, and the R/W control line, as illustrated in Table 3.7. The MT8952's registers can be grouped into three general categories, namely:

- status registers, which are read only;
- control registers, which are read and write;

- and receive and transmit registers, which can be read and/or write.

Table 3.8: MT8952 FIFO: Received Byte Status

BITS 7-6	STATUS
'0 0'	Packet Byte
'0 1'	First Byte
'1 0'	Last Byte - Good FCS
'1 1'	Last Byte - Bad FCS

The FIFO Status Register contains four two bit groupings which indicate the status of the receive and transmit FIFOs. Received Byte Status, bits 7 and 6, denote the status of the byte ready to be read from the receive FIFO, as illustrated in Table 3.8.

Table 3.9: MT8952 FIFO: Receive FIFO Status

BITS 5-4	STATUS
'0 0'	Receive FIFO Empty
'0 1'	Less than or equal to 14 bytes
'1 0'	Receive FIFO Full
'1 1'	Greater than or equal to 15 bytes

The Receive FIFO Status bits 5 and 4 reflect the buffer availability status of the receive FIFO itself, as depicted in Table 3.9. The Transmit FIFO Status bits 3 & 2 designate the buffer availability status of the transmit FIFO, examplified in Table 3.10, while bits 1 & 0 are unused and held low.

Transmit and receive FIFO status bits are not updated immediately after reads or writes from the serial and parallel ports. The updates are delayed after two or four falling edges of the clock signal, which is dependent upon the timing mode. In

Table 3.10: MT8952 FIFO: Transmit FIFO Status

BITS 3-2	STATUS
'0 0'	Transmit FIFO Full
'0 1'	Greater than or equal to 5 bytes
'1 0'	Transmit FIFO Empty
'1 1'	Less than or equal to 4 bytes

the internal timing mode of this design four C4i falling edges must pass prior to the update.

Table 3.11: MT8952 General Status Register Bit Definitions

BIT#	NAME	DESCRIPTION
7	Rx OVFL	Receive FIFO Overflow: '1' – all subsequent bytes lost
6	Tx URUN	Transmit FIFO Underrun: '1' – abort packet being transmitted, clear by reading the Interrupt Flag Register
5	GA	Go Ahead: '1' active – detects frame flag, clear by reading IFR
4	ABRT	Abort: '1' active – detects flag in data, clear – read GSR
3	IRQ	Interrupt Request: indicates compliment of IRQ(low) pin
2	IDLE	Idle Channel: '1' active – idle channel detected on CDSTi
1-0	Unused	set to '0'

The C-Channel Status Register continuously stores data received in the channel 1 timeslot of the incoming ST-BUS (CDSTi). The General Status Register is outlined and defined in Table 3.11.

The final status register is the Interrupt Flag Register, and is represented in Table 3.12. Some bits in other registers can only be cleared by reading this register. Setting the appropriate bits in the Interrupt Enable Register allows the IRQ pin to go low, signaling the PC of an interrupt. Bit assignments are identical to the Interrupt Flag Register.

Table 3.12: MT8952 Interrupt Flag Register

BIT#	NAME	DESCRIPTION
7	GA	Go Ahead: '1' – go-ahead sequence, on DSTi
6	EOPD	End Of Packet Detect: '1' – end of packet, packet aborted, or bad packet
5	TxDONE	Transmitter Done: '1' – packet transmit complete and FIFO is empty
4	FA	Frame Abort: '1' – frame abort detected on CDSTi
3	TxFULL	Transmit FIFO 4/19 FULL: '1' – only 4 of 19 bytes in use in FIFO (15 available)
2	TxURUN	Transmit FIFO Underrun: '1' – FIFO is empty and no end of packet detected
1	RxFULL	Receive FIFO 15/19 FULL: '1' – only 4 available bytes in FIFO (15 are full of data)
0	RxOVFW	Receive FIFO Overflow: '1' – FIFO is full, all subsequent bytes are discarded

Table 3.13: MT8952 Control Register Bit Definitions

BIT#	NAME	DESCRIPTION
7	TxEN	Transmit Enable: '1' – enables transmitter '0' – high impedance packet by packet control
6	RxEN	Receive Enable: '1' – enables receiver, '0' – disables receiver packet by packet
5	RxAD	Receive Address: '1' enables unique address detection
4	RA6/7	Receive Address 6/7: '1' – address is upper 6 bits '0' – address is upper 7 bits of address byte
3-2	IFTF	Interframe Time Fill: designates active and idle states '0 0' – idle state (all ones) '0 1' – Interframe Time Fill state (continuous flags) '1 0' – Transparent data transfer '1 1' – Go Ahead state (continuous 7F(hex))
1	FA	Frame Abort: '1' – marks frame & transmits abort sequence
0	EOP	End Of Packet: '1' – tags next byte as end of packet

The C-Channel Control Register allows the PC or microprocessor to write to the output stream on CDSTo when in internal timing mode. In effect it acts as a parallel shift register interfacing two ports. Data is transmitted in the channel 1 timeslot.

Table 3.14: MT8952 Timing Control Register

Bit#	NAME	DESCRIPTION
7	RST	Reset: '1' – all registers are reset and FIFOs cleared
6	IC	Internal Control: '1' – internal timing, '0' – external timing when '0' – transmit and receive are enabled through the TxCEN and RxCEN pins
5	C1EN	Channel 1 Enable: '1' – control on channel 1, '0' – channel one set to high impedance
4	BRCK	Bit Rate Clock: '1' – external clock is C2i (low), otherwise, if '0' – external clock is C4i (low)
3-0	TC	Timing Control Bits: used in internal timing mode transmit and receive sections enabled as follows
		'X 0 0 0' – Channel 0 – 1 bit per frame 'X 0 0 1' – Channel 0 – 2 bits per frame '0 0 1 0' – Channel 0 – 6 bits per frame '1 0 1 0' – Channel 0 – 7 bits per frame 'X 0 1 1' – Channel 2 – 8 bits per frame 'X 1 0 0' – Channel 3 – 8 bits per frame 'X 1 0 1' – Channel 4 – 8 bits per frame 'X 1 1 0' – Channels 2 & 3 – 16 bits per frame 'X 1 1 1' – Channels 2, 3 & 4 – 16 bits per frame

The Timing Control Register controls the timing mode and related operations, providing a software reset to the Protocol Controller. Bit format, functions, and function definitions are outlined in Table 3.14, below. The design requires internal timing (bit six set to one).

The PC communicates with the DNICs via the Receive Data and Transmit Data registers. The Controller and DX send and receive the LSB first while the DNIC

sends and expects the MSB first. Therefore care must be taken with the software. Reading the Receive Data Register puts the first byte of the receive FIFO on the PC or microprocessor's data bus, with the least significant bit being D0. Writing to the Transmit Data Register puts one byte of data at the end of the transmit FIFO. This byte will be transmitted serially D0-D7. The LSB in the Receive Address Register is always low, while the remainder of the bits will designate the destination address of the incoming packet. Valid addresses are composed of either six or seven bits as designated by bit four of the Control Register.

Writing 'XXX0 1010' to the Watchdog Timer Register resets the Watchdog Timer, which is an eleven stage binary counter with $\overline{F0i}$ as the input and $\overline{WD}$ as the output. Four milliseconds, 1024 cycles, after reset, the timer outputs a low signal for 4 ms or until it is reset again on pin $\overline{WD}$.

ST-BUS Transmit Operation After power up reset and prior to enabling the transmit section with the TxEN bit of the Control Register, timing should be set to internal mode via the Timing Control Register. The TCR C1EN bit should also be set to initiate conversation with the DNICs via C-channel, channel-1, transmission.

Beginning with the address, data can be written to the Transmit Data Register for transfer. The IFTF bits in the Control Register must not be set to '1 1', the Go Ahead state, for transfer to begin. The last byte of the packet must contain the EOP bit for the packet to be valid, otherwise the Controller will flag a transmit underrun, TxURUN.

ST-BUS Receive Operation After reset the receiver should be enabled similar to the transmitter. If incoming address detection is desired, the RxAD bit in the

Control register must be set to one. Invalid packets of less than 24 bits are discarded, and packets of 32 bits are tagged as having a bad FCS. Aborted packets are flagged and removed from the FIFO. The GA sequence can be programmed to initiate an interrupt. Finally receiver FIFO overflow can and should be set up to interrupt the PC. All data is read from the Receive Data Register.

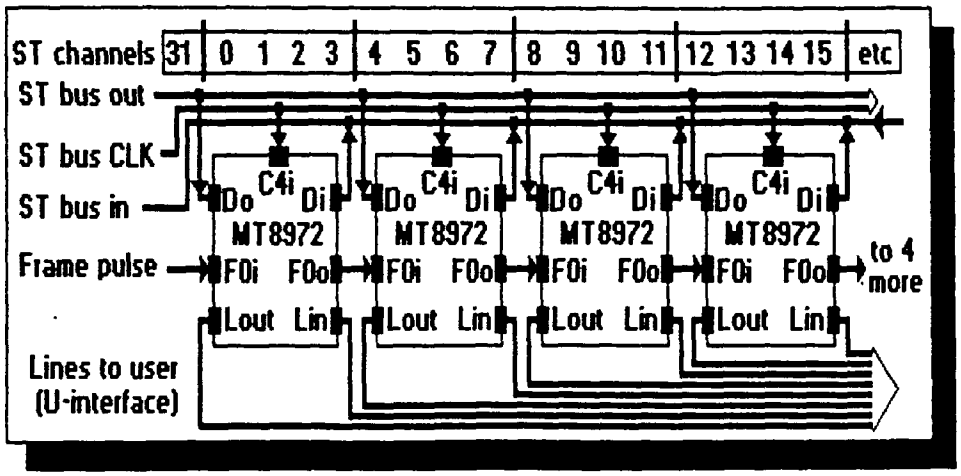


Figure 3.10: DNIC Daisy-Chain Diagram

DNIC Daisy-Chaining The MITEL ST-BUS can support up to eight DNIC's or SNIC's, MITEL's T-Interface chip, for maximum bus bandwidth utilization via daisy-chaining of the devices. The primary advantage of daisy-chaining DNIC's, however, is that each DNIC does not require a separate HDLC Protocol Controller. Using one Protocol Controller minimizes the hardware design and its cost. This approach is much more software intensive.

The original design contained four daisy-chained DNIC's, as illustrated in Figure 3.10. Each were assigned four successive channels on the ST-BUS via the $\overline{F0i}$ frame pulse timing. The signal is passed to the next DNIC in the chain via $\overline{F0o}$ at the end of a DNIC's frame period of four channels or 32 bits. The 4th DNIC in the chain does not return the the signal to the 1st, however. This allows the last 16 channels to go to high impedance. Only the first 16 channels are divided into timeslots for use by the DNICs.

ST-BUS Data Flow Primary Rate Interface channels arrive at the DX at STi3, as illustrated in Figure 3.1. Channels whose destination addresses are one of the DNICs will be referred as local. Non-local addresses should be routed back to the trunk via STo3; The remaining data flows as follows:

- all DNIC incoming D, C, and B channels arrive at the DX at STi1 in that order and in each DNIC's respective timeslot;
- remotely addressed channels are output on channel STo3;
- all incoming, locally addressed B channels are output on STo1;
- all incoming DNIC D-channels are routed to the Protocol Controller via channel 0 of STo2 at predetermined regular intervals;
- D-channels originating at the Protocol Controller arrive at STi2 on channel 0, and are routed to the respective DNIC via STo1;
- and C-channel communication between the PC and the DNICs passes through the DX via STi1 and STo1 on channels 1, 5, 9, and 13, when the DX is set up to put those channels into message mode. PC access is via the DX's parallel port.

Each DNIC is active only in its assigned timeslot. When a D-channel is inactive an all '1's' pattern is transmitted in the assigned D-channel slot. If the PC wishes to transmit a packet, it connects channel 0 of STi2 to the desired DNIC's channel at STo1. For polling and GA sequence interrupts the PC connects each D channel of STi1 to channel 0 of STo2 for a period of one millisecond. The Controller will then listen to this channel for an incoming message. The DNIC will transmit a GA

sequence which the PC acknowledges during the interrupt handler. The DNIC may then begin to transmit.

As mentioned earlier this method is software intensive and should not be used where a high volume of traffic is expected, or where system response time is critical. If such conditions are anticipated, DNICs should be matched each to a Controller, or the software required to control the data flow should be implemented in hardware.

Testing the PC Board

This design tested to be non-operational due to:

- The IBM XT was not fast enough to perform HDLC and switching functions.
- All hardware components for the PRI were not available, namely the MT89761, a MITEL T1 Digital Trunk Transmit Equalizer.
- The Layer 3 software was not written for the PC until the fall semester, 1990.
- The addition of the software to the overloaded PC was not feasible.

CHAPTER 4. THE REVISED DESIGN OF THE CENTRAL OFFICE

Project Goals

Revised Goals

As a result of the inadequacies of the original design, the design approach was reevaluated, and the goals revised. The revised goals included:

1. Retain Layer 1 and Layer 2 functions in hardware and Layer 3 functions in software;
2. Implement distinct functions, interfaces, on separate cards, as follows:
   (a) Move the U-Interface from the original PC board to a separate board.
   (b) Retain as much of the original PC board design as possible namely:
      i. the timing circuitry;
      ii. the main switch;
      iii. the PC bus interface circuitry;
      iv. and the incomplete PRI circuitry;
   (c) Add S/T interface capabilities on a separate PC board;
3. Add microprocessors to the interface cards to solve the PC speed problem.

4. Move some of the call control and circuit setup software into ROM for the microprocessors to handle.

5. Isolate the user physical accesses outside the PC on a special card.

Added Goals

With the formal acceptance of the 2B1Q signaling standards by the CCITT at the U-Interface and the potential market demand for a PC-based central office on university campuses, two additional goals were formulated during the design process. The first of these was to develop formal detailed schematics of the design such that boards could be developed and built commercially. Secondly, changes to the present U board design were needed to comply with the 2B1Q signaling standard, because the MT8972's did not fulfill the standard's requirements. The required changes needed to be outlined in detail.

Division of the Design Project

With the expansion and changes to the original design, the project was divided into three subprojects, and assigned to graduate students in the Computer Engineering Master's program as follows:

1. The design and testing of the S/T-Interface card was assigned to Angela Bradley.

2. The design and testing of the U-Interface card was assigned to Timothy Toillion.

3. The design, revision, implementation, and testing of software was assigned to Suresh Dongre.

Typical Operation of a Central Office

Possible Connections

When completed the Central Office will be responsible for establishing, maintaining, and terminating connections of users that may be interfaced to the office via separate distinct interfaces or a common interface. The connection request may be local, over either the basic rate T-Interface or U-Interface, or remote, over the PRI. Nine distinct possible connections are:

1. U-Interface to U-Interface, which is is routed through the main switch back to the U-Interface card.
2. U-Interface to T-Interface, which is routed through the main switch.
3. U-Interface to remote, which is routed through the main switch and PRI.
4. T-Interface to T-Interface, which is routed through the main switch back to the T-Interface card.
5. T-Interface to U-Interface, which is routed through the main switch.
6. T-Interface to remote, which is routed through the main switch and PRI.
7. remote to T-Interface, which is routed through the main switch and handled on the T-Interface card.
8. remote to U-Interface, which is routed through the main switch and handled on the U-Interface card.
9. remote to remote, which is routed through the main switch and PRI.

Interactions

A typical voice call connection from a user on the T-Interface to a user on the U-Interface will exemplify the interactions within the central office. Data connection establishment and termination and voice connection termination cause a similar set of events. Steps for a voice call connection are [6]:

1. The caller alerts the TE that a connection is requested, picks up the digital telephone handset.

2. The TE sends a LAP-D packet with Q.931 information requesting a call setup to the central office via the T-Interface board.

3. The microprocessor on the board is interrupted, fetches the packet from the SNIC, decodes the message, and returns a go-ahead to the TE via the SNIC.

4. The TE then sends the address of the called party via digits entered.

5. The microprocessor fetches the address and writes it into the Dual-Port RAM.

6. The microprocessor sends an interrupt to the PC.

7. The PC reads the address from Dual-Port RAM, checks its routing table, sets up a route via the main switch, sends the options requested, and checks the status of the caller's line for an available B channel.

8. The PC writes the status information into Dual-Port RAM and interrupts the microprocessor on the T-Interface board.

9. The microprocessor reads the reply from Dual-Port RAM, waits for an available B channel, and sends a call proceeding packet to the TE via the SNIC.

10. Simultaneously the TE alerts the caller of the call's status, and the the U-Interface board's microprocessor alerts the called party's TE of an incoming call via the HDLC Protocol Controller and DNIC.

11. When the called party responds the connection is established.

Overview of the Hardware Design

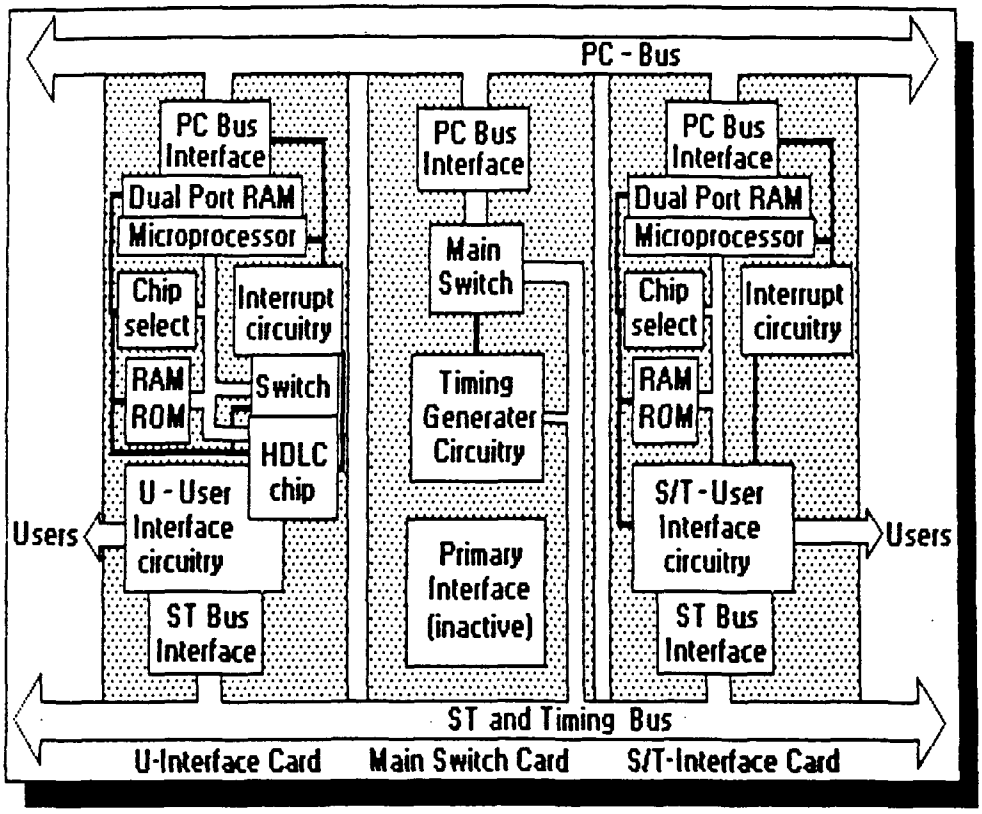


Figure 4.1: Central Office Block Diagram

The present design of the ISU ISDN central office consists of an IBM XT PC with three additional internal PC boards, cards, and an external user access board.

In addition to the PC bus, the three PC boards are connected by a Timing/ST-BUS ribbon, as depicted in Figure 4.1.

T-Interface and U-Interface cards contain Motorola MC6809 bus based systems. The Motorola MC6809 was chosen for the two interface PC boards because it was recommended by MITEL as the simplest interface to MITEL's ISDN chips. These control the MITEL components and interface to the PC via a dual-port RAM. At present the main switch card has no microprocessor based subsystem. Each PC card possesses distinct functionality for optimal expandability of the design.

The Main Switch Card

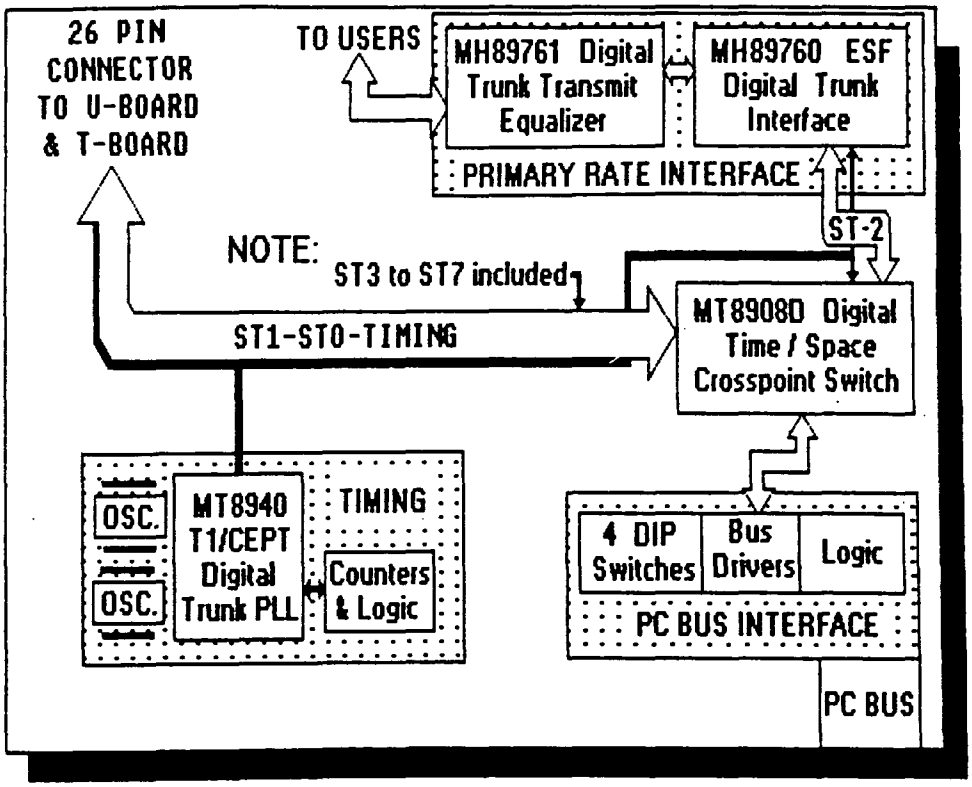


Figure 4.2: The Main Switch Card Block Diagram

The U-Interface circuitry was removed from the original design, leaving the DX, an inactive PRI, timing circuitry, and the PC bus interface circuits. The splitting of the design required the addition of a Timing/ST bus connector and interface, as illustrated in Figure 4.2. The circuits removed were the four DNICs, the Protocol Controller, and the user access resistors, capacitors, and transformers.

The External Board

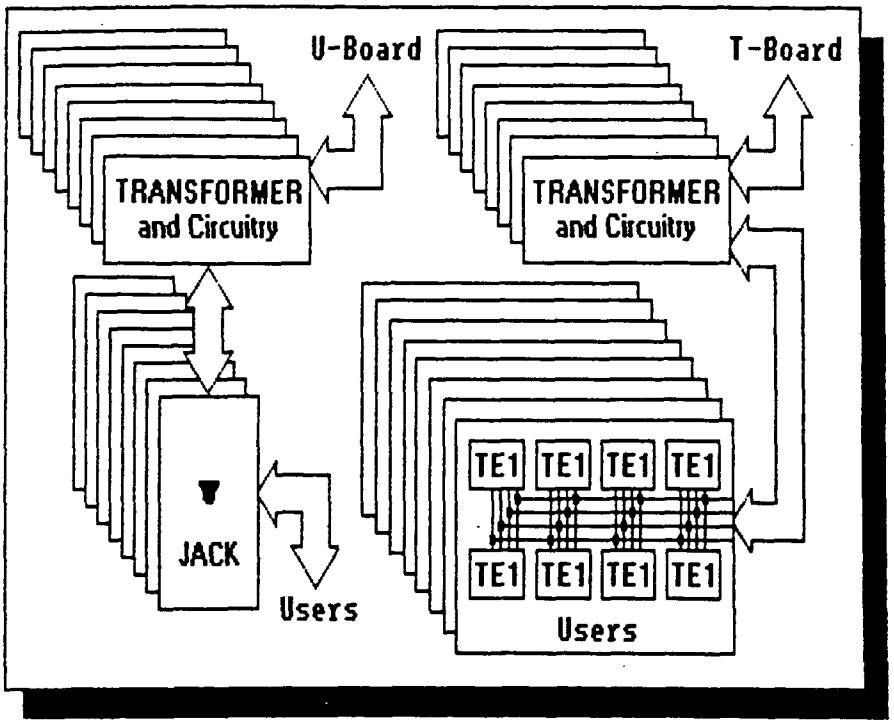


Figure 4.3: The External Board Block Diagram

The user access board will contain 16 transformers and jacks, together with the circuitry required to interface to the SNICs and DNICs, as illustrated in Figure 4.3. A total of 24 twisted pairs, or 48 wires will be needed off board. Four wires are required for each SNIC and two wires are required for each DNIC. Each SNIC can

support a passive bus containing as many as eight pieces of terminal equipment.

The S/T-Interface Card

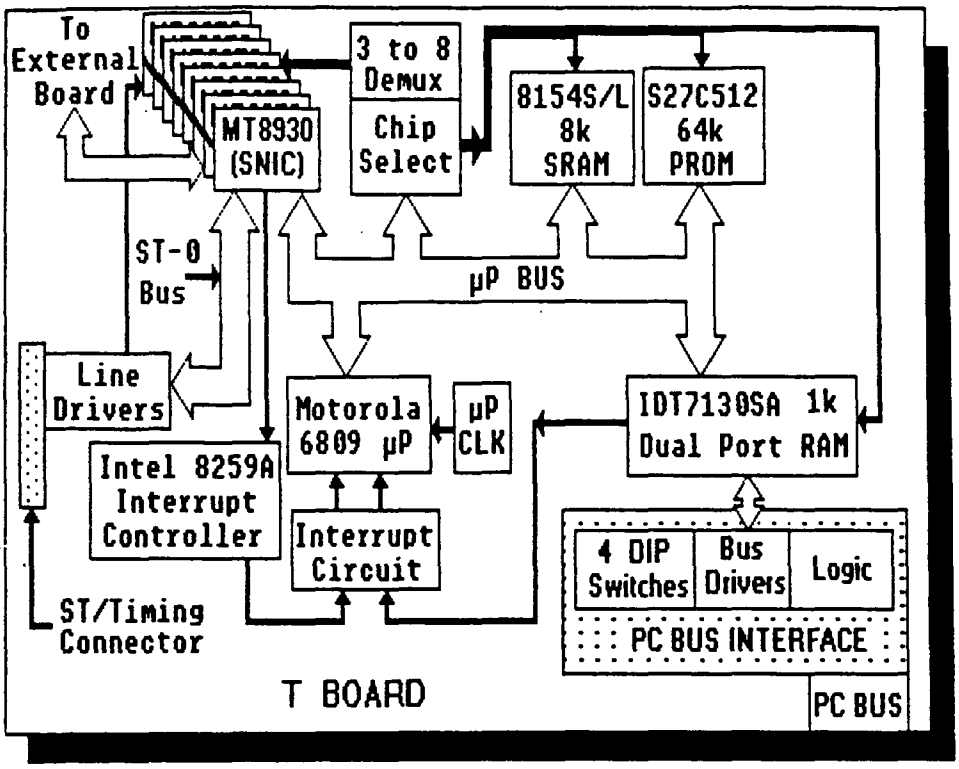


Figure 4.4: The T-Interface Card Block Diagram

The T-Card provides network termination functions to its users and is depicted in Figure 4.4, above. The T-Card consists of five major functional parts, which are:

- The PC-BUS interface, which not only includes the addition of a Dual-Port RAM, but also requires more logic than the original board.
- The ST-BUS and timing interface which consists of a ribbon connector and drivers.

- The Motorola MC6809 bus system including RAM and ROM.
- Eight daisy-chained SNICs providing the T-Interface and network termination functions.
- Finally, a control interface for Motorola bus components and SNICs, which consists of interrupt and chip select logic.

The bus interfaces, the microprocessor system, and most of the control logic is similar to the U-Card's and will be detailed in the following chapter. The distinct components of the T-Card are the SNICs, the 8259A Interrupt Controller, and the chip select control for the SNICs.

The MT8930 Subscriber Network Interface Circuit

The primary features of the SNIC include [19]:

- CCITT I.430 S and T interface via two twisted pairs;
- Full duplex 2B + D (basic rate), 192 kbps pseudo-tenary signaling transmission;
- Choice of point-to-point, point-to-multipoint, and star configurations;
- Master/Slave modes of operation;
- Complete loopback testing capabilities;
- Self contained timing extraction via on chip PLL.
- HDLC (LAPD) D-channel protocoller;
- Eight bit parallel port, for microprocessor interfacing;

- MITEL ST-BUS interface;
- Low power CMOS technology;
- Single 5 Volt power supply;

The User Interface The SNIC supports pseudo-tenary signaling, alternate zero inversion (AZI) [6], at the line connections, as described in Chapter 2. D-channel access contention resolution via echo bit monitoring is supported for up to eight pieces of terminal equipment. The star configuration, or extended bus, is a variation from CCITT standards, but does not affect operation.

SNIC Daisy-Chaining Eight SNICs are daisy-chained in the same way as the DNICs in the original design. ST-BUS timeslot allocation requires all 32 channels, four for each SNIC. As in the original design allocation is achieved with the $\overline{F0i}$ and F0b(low) frame pulse signals. The channel order and functions are identical. $\overline{C4i}$ is used for bit timing.

The Microprocessor Interface Unlike DNICs that interface to the MC6809 via the HDLC Protocol Controller, SNICs interface directly to the microprocessor.

Eight of the bidirectional parallel port's pins are used for addressing and transfer of data. This requires the use of an address buffer on the bus. Otherwise, the functionality provided to the microprocessor is comparable to the MT8952 HDLC Protocol Controller's, which was detailed in Chapter 3. The SNIC contains sixteen registers used for control, status monitoring, and sending data by the microprocessor. Transmit and receive operations are handled in a similar manner as the MT8952

HDLC Protocol Controller.

The size of the transmit and receive FIFOs are identical to the MT8952's FIFOs. The major advantage here is that each of the eight SNICs contains the same amount of buffer space as is available to all eight of the daisy-chained DNICs. Protocol Controller. The major disadvantage occurs in interrupt control and chip select requirements.

SNIC Interrupt Control

Since the MC6809 has only three interrupt pins and must be able to identify the source of the interrupt from nine possible devices, the SNICs and the PC interface, the Intel 8259A Interrupt Controller was chosen to provided the SNIC interrupt interface to the MC6809. The SNIC IRQ pins are tied in order to the 8259A's parallel input register's. When an SNIC generates an interrupt to the 8259A, it responds by generating an interrupt to the MC6809, which in turn addresses the 8295A and reads its status register via the MC6809 bus.

The Intel 8259A Interrupt Controllers can be cascaded to handle two to the power eight or 64 devices. However, one MC6809 could become overwhelmed if 64 SNICs were used.

S/T-Card Memory Mapping

The MC6809 supports 64k byte addressing with 16 address lines and 8 data lines. Although the memory mapping on the T-Card and U-Card is the same. The number of devices accessed via memory mapping are different. Since there are eight SNICs to address a 3 to 8 demultiplexer is used on this board to provide the chip

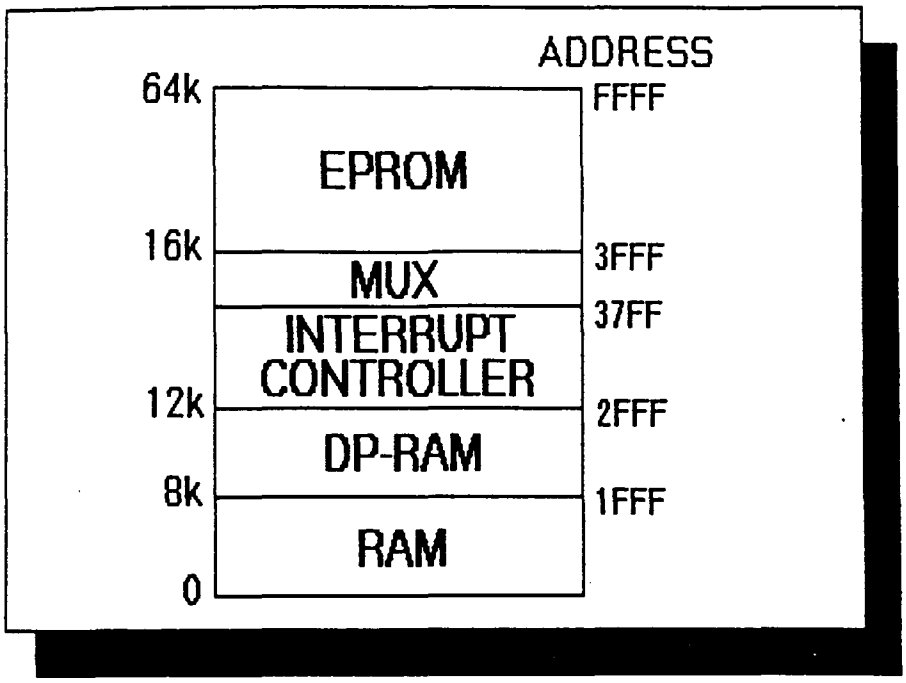


Figure 4.5: S/T Card Memory Mapping Diagram

select signals. A PAL is used to provide chip select signals to the EPROM, RAM, Dual-port RAM, Interrupt Controller, and the demultiplexer. The memory mapping is depicted in Figure 4.5.

The Microprocessor System

Details of the U-Card's microprocessor system, PC bus interface, and ST-BUS interface are provided in Chapter 5. These closely resemble the T-Card's. The U-Interface itself nearly mirrors the original design, as presented in the preceding chapter.

CHAPTER 5. THE DETAILED DESIGN OF THE U-INTERFACE PC BOARD

General Hardware Design Changes

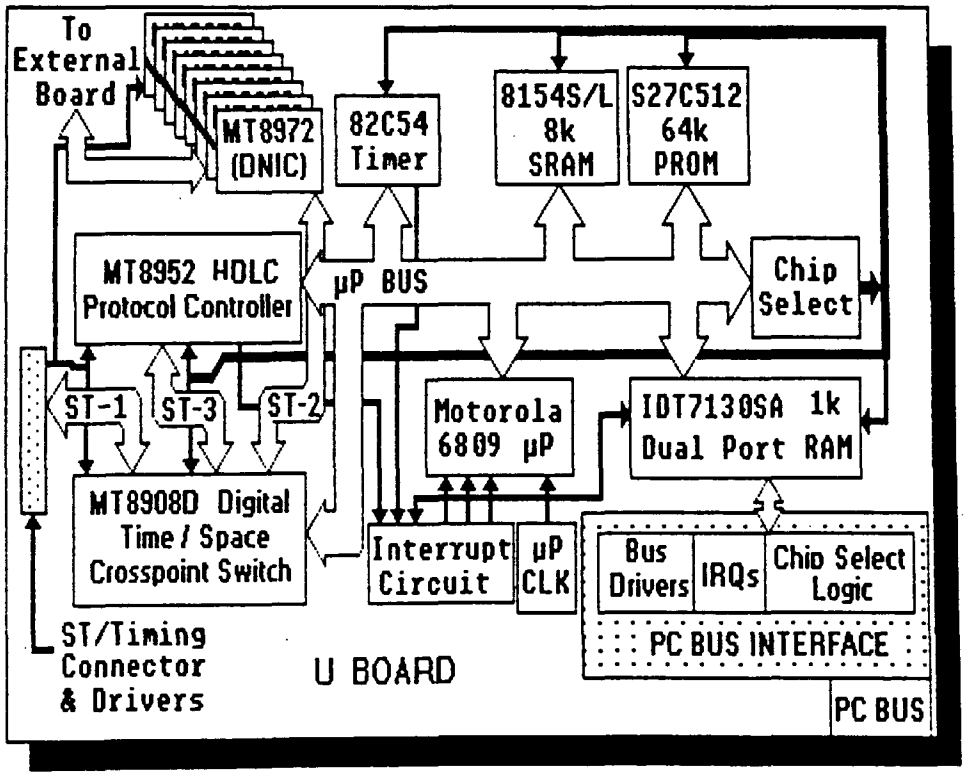


Figure 5.1: The U-Card Block Diagram

Design of the U-Interface PC board, U-Card, illustrated in Figure 5.1, was based upon the original central office design's implementation of the U-Interface, with the

following additions:

- The number of daisy-chained DNICs was increased to eight.
- The number of ST-BUSes and connections to the DX was increased to four to accommodate routing to and from the main board.
- An MC6809 microprocessor system, including RAM and ROM, was added to:
  - implement LAP-D and Q.931 protocols previously handled by the PC,
  - facilitate the control requirements of the DNICs via the HDLC Protocol Controller,
  - and provide routing via the DX.
- An IDT7130 Dual-Port RAM, complete with interrupts, was added to the PC bus interface to act as a bidirectional mailbox, buffer of information.
- A ribbon connector and interface was added to support eight ST-BUSes and ST-BUS timing.
- An INTEL 8254 Programmable Interval Timer was added to the microprocessor bus to facilitate one millisecond timeouts signaling the microprocessor to switch the next D-channel via the DX to the Controller.

U-Interface Operation

Component Interaction Changes

The functionality and interaction of the U-Interface components, the DX, DNICs, and Protocol Controller was detailed in Chapter 3. The MC6809 system replaces the

PC. Eight daisy-chained DNICs require all 32 ST-BUS channels instead of 16. The only addition to the functionality of the U-Interface components that deviates from the original design is the Interval Timer's role.

Additional Functionality

The Interval Timer is used to generate an interrupt one millisecond after it is set. This represents the timespan, two bits per frame for eight frame pulses of 125 milliseconds each, required by the HDLC Controller to detect a go-ahead sequence on each DNICs D channel. The go ahead sequence is nine bits long with a shared '0' between sequences, and is generated by a TE through the DNIC when the TE desires to send.

Upon receiving a go-ahead sequence the Controller sends an interrupt to the microprocessor so the request can be processed. The Timer interrupt directs the MC6809 to switch the next DNICs D channel to the Controller's channel 0 to poll the device. The timer must be reset after each timeout.

INTEL 8254 Programmable Interval Timer

Description The Timer is very flexible containing three counters of 16 bits each, a control and status register, and five uniquely distinct modes of operation that may be programmed separately for each counter. Each counter can be clocked separately, allowing the output of one counter to be used as an input to another counter or to generate an interrupt. Counters may be individually operated as binary or BCD counters. Control Register bits are defined in Table 5.1. One problem interfacing to the MC6809 is that reads and writes are done on separate pins, both

Table 5.1: 8254 Interval Timer Control Register

BIT#	NAME	DESCRIPTION
7-6	SC	Select Counter: by binary value '1 1' is read back
5-4	RW	Read/Write: '0 0' – Counter Latch Command '0 1' – R/W least significant byte '1 0' – R/W most significant byte '1 1' – R/W least first then most significant byte
3-1	M	Mode: 5 modes by binary value, mode 0 is interrupt
0	BCD	'1' is BCD – '0' is binary

asserted low. To solve this an inverter is connected to the read.

Operation

This design uses one counter clocked by ST-BUS frame pulse $\overline{F0i}$ The status of the counter can be read without affecting the count. The count may be stopped by latching the gate pin low and initiated by latching the gate pin high. The gate input is an edge sensitive flip-flop sampled on the rising edge of the clocks. Any write, except writing to counter 0, will latch the gate low and disable the interrupt in this design. Writing '07' hex to counter 0 will produce the one millisecond interrupt. If the top byte is initialized to '00', only the lower byte need be written to.

Initialization

At power up the Timer's state is undefined, therefore it must be initialized. Counters are initialized by writing a Control Word and then an initial count, which is written to the desired counter or counters. The counter is initialized as a binary counter in mode 0, interrupt on terminal count, in this design. Counters are addressed

via A1 and A0 pins by binary value. Both pins high address the control register. The count written to counter 0 should be followed by a write to another counter or an interrupt will be generated.

The ST-BUS Interface

The 26 Pin Ribbon Connector

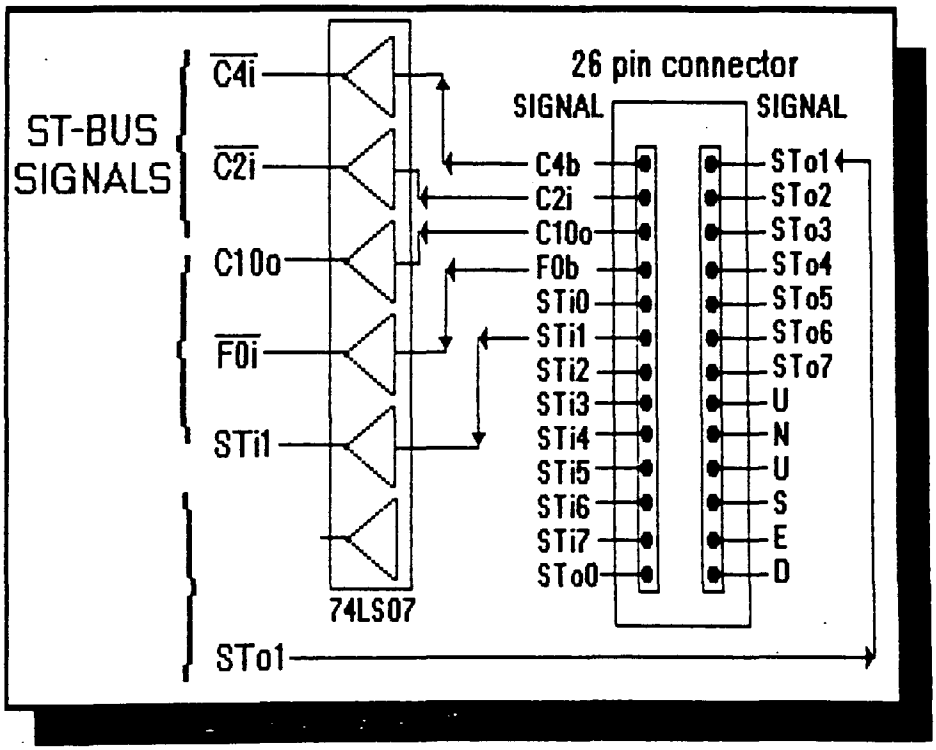


Figure 5.2: The ST-BUS Interface Block Diagram

All cards in the design share access to the ST-BUS ribbon cable, consisting of 20 active lines as depicted in Figure 5.2. All timing signals originate from the Main Switch Card, and presently only two of the ST-BUS pairs are used. ST connects the main DX with the T-Card and ST connects the main DX to the DX on the U-Card.

The remaining lines are for future expansion.

The Interface Circuit

All incoming line signals are routed through 74LS07 drivers to strengthen their respective signals. The delay introduced by these drivers coupled with line delay, may create the need to delay timing signals on the Main Switch Card.

The PC-BUS Interface

The PC-BUS Pin Assignments

The PC board's 64 pins plug into the PC-BUS. Pin assignments are illustrated in Figure 5.3. Not all of the pins are used in the interface. The pins used are:

- A19-A10 enable the chip select on the Dual-Port RAM via a logic circuit.
- A9-A0 are buffered and address memory locations in the Dual-Port RAM.
- D7-D0 are used to transfer data.
- $\overline{MEMR}$ & $\overline{MEMW}$ are used to read from and write to the Dual-Port RAM.
- I/O CH RDY connects to the $\overline{BUSY}$ on the Dual-Port RAM.
- IRQ5 connects to the $\overline{INTR}$ on the Dual-Port RAM.

IDT 7130SA/LA Dual-Port RAM

The IDT 7130SA/LA Dual-Port RAM acts as a double mailbox between the PC and the MC6809. It possesses two complete parallel ports. PC bus connections

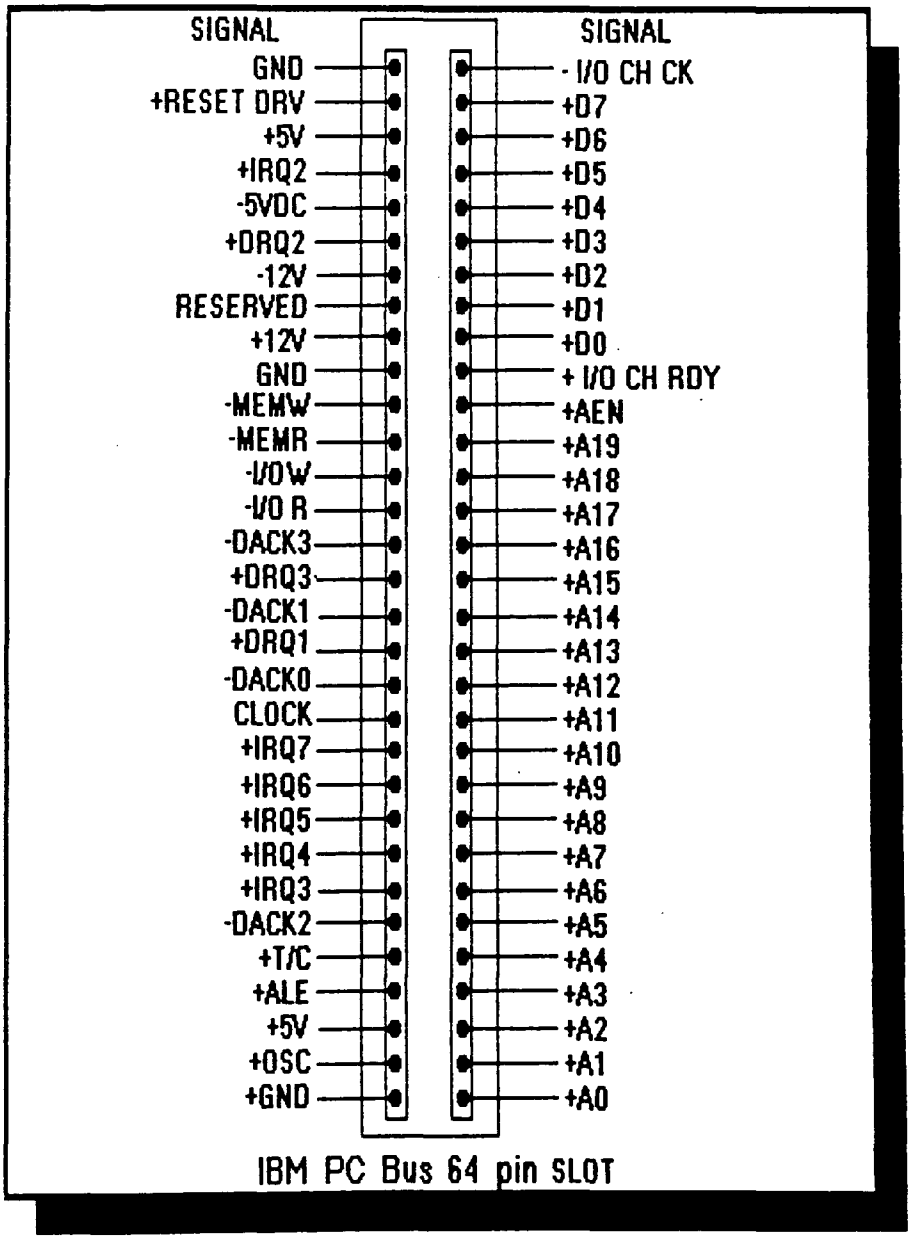


Figure 5.3: PC-BUS Pin Assignments

are given above and similar connections exist on the MC6809 bus, allowing shared access to all memory locations. The interrupts, requiring pullup resistors, perform the required handshaking when the mailboxes are written to. The PC's mailbox is written to by the MC6809 at memory location 3FF on the chip, while the MC6809's mailbox is memory location 3EF. The interrupt is cleared when the mailbox is read [10].

Contention for the same memory location is resolved within the Dual-Port Ram by the arbitration unit. A $\overline{BUSY}$ flag is set for the port denied access. This interfaces to the PC via the I/O CH RDY pin, and to the MC6809 via the MRDY pin.

Supporting Circuits

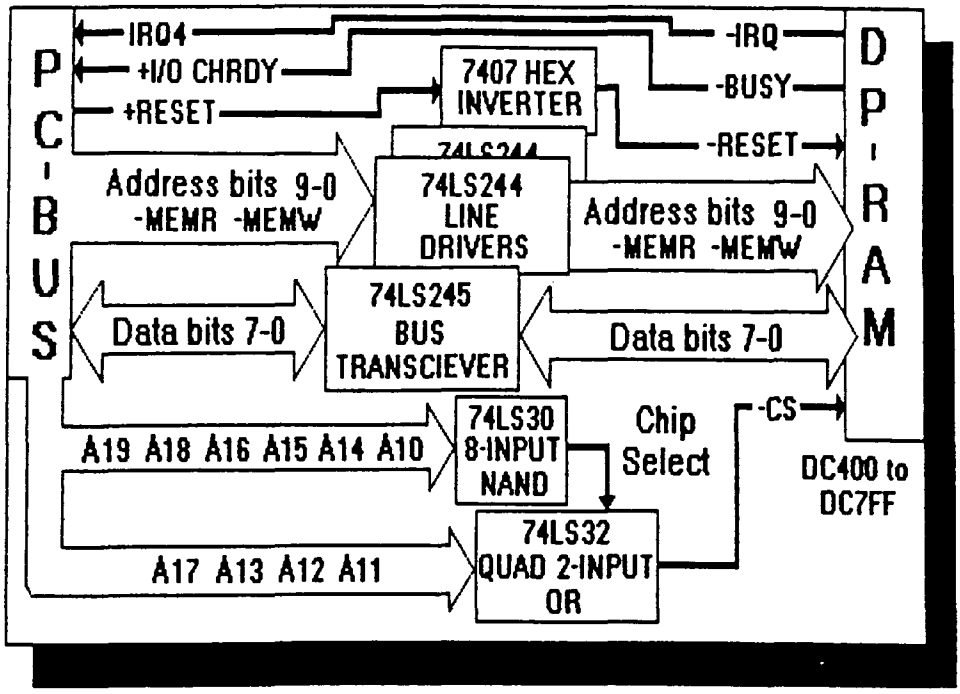


Figure 5.4: The PC-BUS Interface Block Diagram

Besides the circuitry diagrammed in Figure 5.3, address chip select is required, as illustrated in Figure 5.4. This produces an effective PC address of DC400 - DC7FF. The S/T card uses the effective address of DC000 - DC3FF inverting A10. The MC6809 accesses the Dual-Port RAM via addresses 2000-23FF on both boards.

The Microprocessor System

The MC6809

The MC6809 is a NMOS 8-bit microprocessor with a cycle time of 125ns. The MC6809's timing is derived from a crystal attached to XTAL and EXTAL, pins 39 and 38 respectively, and is separate from the ST-BUS timing. Its 16 address lines allow up to 64k bytes of memory on the bus.

Registers Five 16-bit and four 8-bit registers are provided in the 6809, as depicted in Figure 5.5. Register D is a pseudo 16-bit accumulator, composed of two 8-bit accumulator registers, A and B. These are used as scratchpad registers and can be accessed as single 8-bit registers, or bytes in the 16-bit accumulator.

The Direct Page, DP, register enhances the direct addressing mode and contains the A15-A8 pin outputs. The Condition Code, CC, register defines the current state of the 6809, as described in Table 5.2.

The 16-bit registers are defined as follows [20]:

- X and Y constitute two indexable 16-bit stack pointers, used to support software stacks queues and buffers;
- Register U is the user stack pointer, used by the programmer to pass arguments

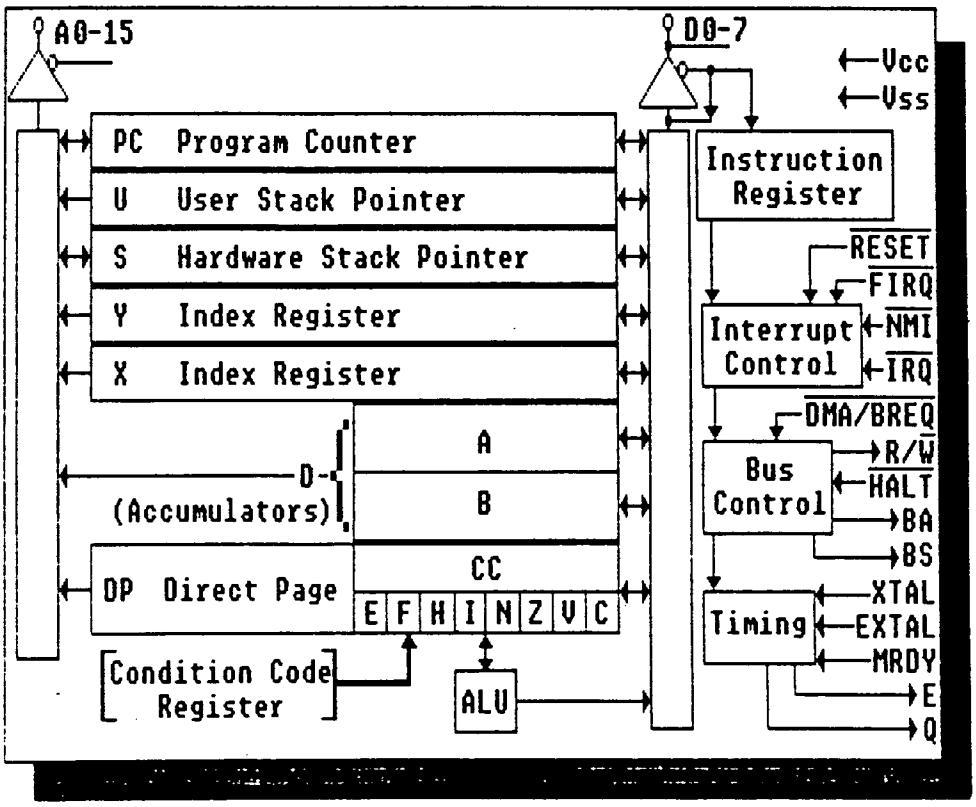


Figure 5.5: MC6809 Registers

Table 5.2: The MC6809 Condition Code Register

BIT#	NAME	DESCRIPTION
7	E	Entire Flag: used on the return call from an interrupt '1' – indicates all registers are stacked '0' indicates the PC and CC were stacked
6	F	FIRQ Mask: '1' – ignore FIRQ interrupts: set by FIRQ, NMI, and RESET
5	H	Half Carry: indicates a carry bit from bit 3 of the ALU
4	I	IRQ Mask: '1' – ignore IRO interrupts: set by IRQ, FIRQ, NMI, and RESET
3	N	Negative Flag: contains the MSB of the result of the last operation: if '1' – indicates last result was negative.
2	Z	Zero Flag: '1' – the result of the last operation was zero
1	V	Overflow Flag: '1' – indicates arithmetic overflow
0	C	Carry Flag: '1' – indicates carry from bit 7 of the ALU

to routines and allowing MC6809 support of high-level languages;

- Register S is the hardware stack pointer used by the MC6809 during subroutine calls and interrupts;
- And the Program Counter stores the address of the next instruction.

Stack pointers point to the top of the stack and not the next free location.

Interrupt Assignments The MC6809 has three hardware interrupts on three separate pins. Non-Maskable Interrupt will be used by the Dual-Port RAM, Fast-Interrupt will be used by the Interval Timer, and Interrupt Request will be used by the Protocol Controller. The $\overline{NMI}$ can interrupt its own handler causing stack overflow. The $\overline{FIRQ}$ stacks only the PC and CC registers and allows fast write operations to the DX and the Interval Timer. The $\overline{IRQ}$ is used when a longer low priority handler is needed, and stacks all of the registers.

Memory

EPROM The Intel 27512 64k byte EPROM stores the program for the MC6809. The lower 16k of it is not addressable, as it occupies addresses 3FFF-FFFF on the MC6809 bus. The $\overline{OE}$ requires an inverted signal from the R/$\overline{W}$ line on the bus to perform a read operation.

To program the EPROM 12V-13V is applied on the $\overline{OE}$/Vpp pin, for one millisecond on the initial programming. If overwriting this voltage needs to be held for a period of up to nearly 79 milliseconds. The only way to de-program the chip is by ultraviolet light erasure.

RAM The Hitachi 6264 8k byte SRAM was used as a temporary scratchpad on the U-Card. The SRAM occupies address space 0-1FFF. It is used to store temporary data by the MC6809, such as bits from the D channel.

Mapping The MC6809 controls and accesses six devices on the U-Card, the EPROM, the DX, the Protocol Controller, the Interval Timer, the Dual-Port RAM, and the SRAM. All devices are accessed via memory mapping, as depicted in Figure 5.6.

PAL Chip Select

A 20 pin 16L8 PAL was used to implement the chip selects. The PAL consists of AND and OR gate array logic, with 8 inputs and 8 outputs available. Six address line inputs were used to generate the required 6 chip select outputs. PAL program files are in Appendix D. The PAL was programmed as follows:

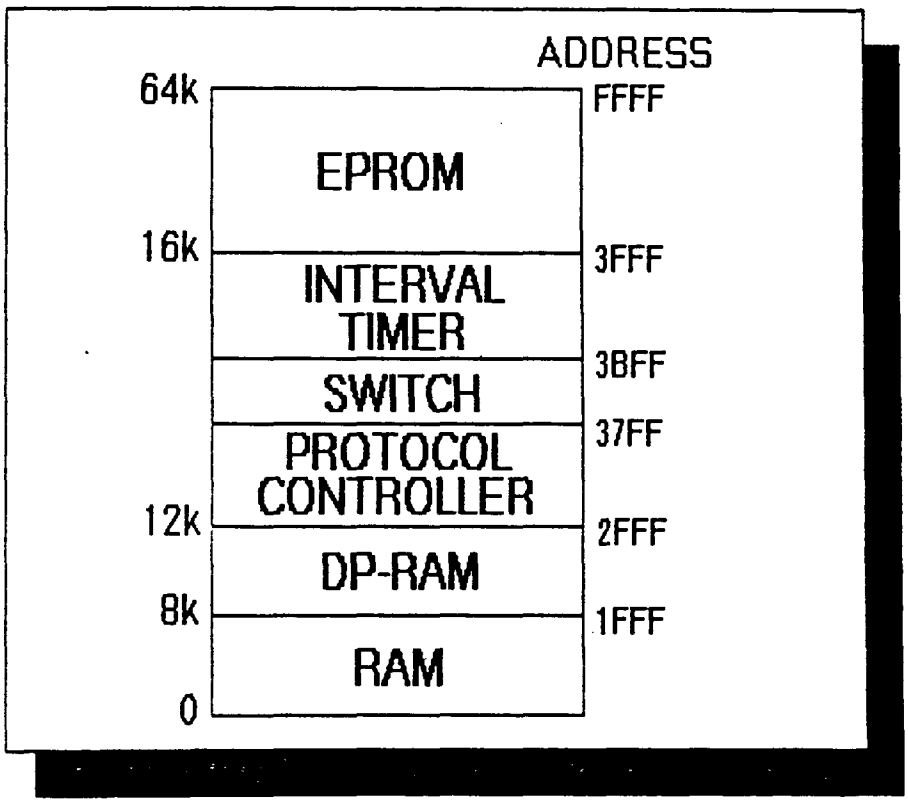


Figure 5.6: U-Card Memory Mapping

- Output 1: (EPROM) = (A15 + A14) (E + Q);
- Output 2: (SRAM) = (E + Q) * ($\overline{A15}$ * $\overline{A14}$ * $\overline{A13}$);
- Output 3: (DP-RAM) = (E + Q) * ($\overline{A15}$ * $\overline{A14}$ * A13 * $\overline{A12}$ * $\overline{A11}$);
- Output 4: (HDLC) = (E + Q) * ($\overline{A15}$ * $\overline{A14}$ * A13 * $\overline{A12}$ * A11);
- Output 5: (DX) = (E + Q) * ($\overline{A15}$ * $\overline{A14}$ * A13 * A12 * $\overline{A11}$);
- Output 6: (Timer) = (E + Q) * ($\overline{A15}$ * $\overline{A14}$ * A13 * A12 * A11);

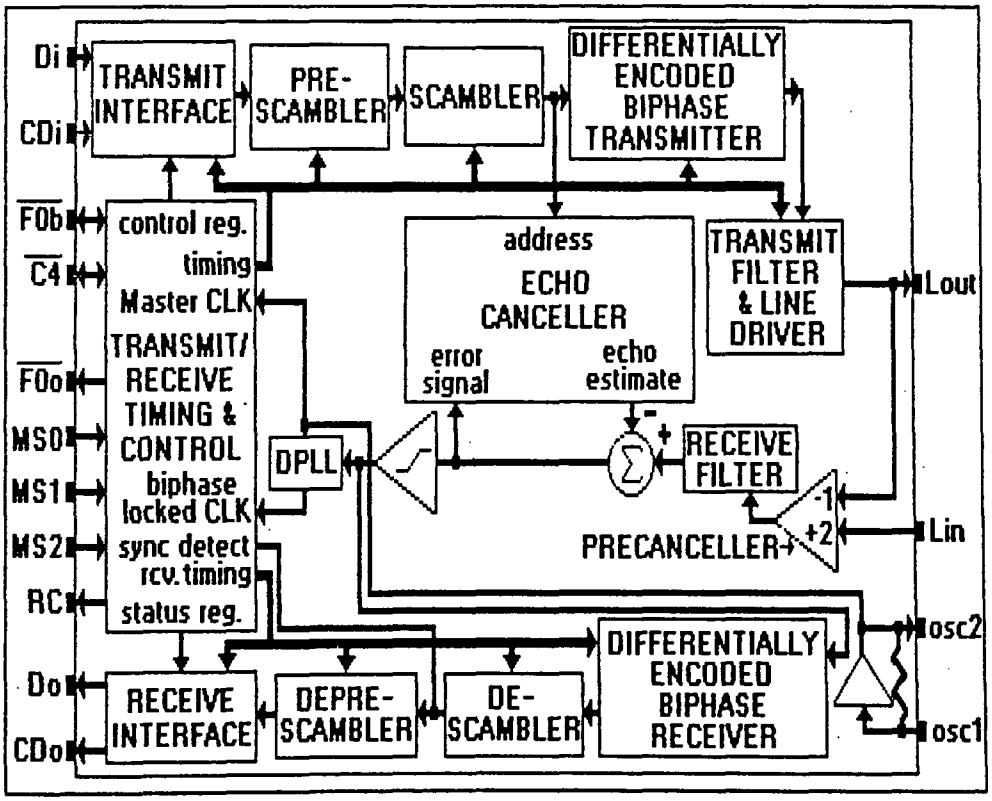


Figure 5.7: MT8972 DNIC Block Diagram

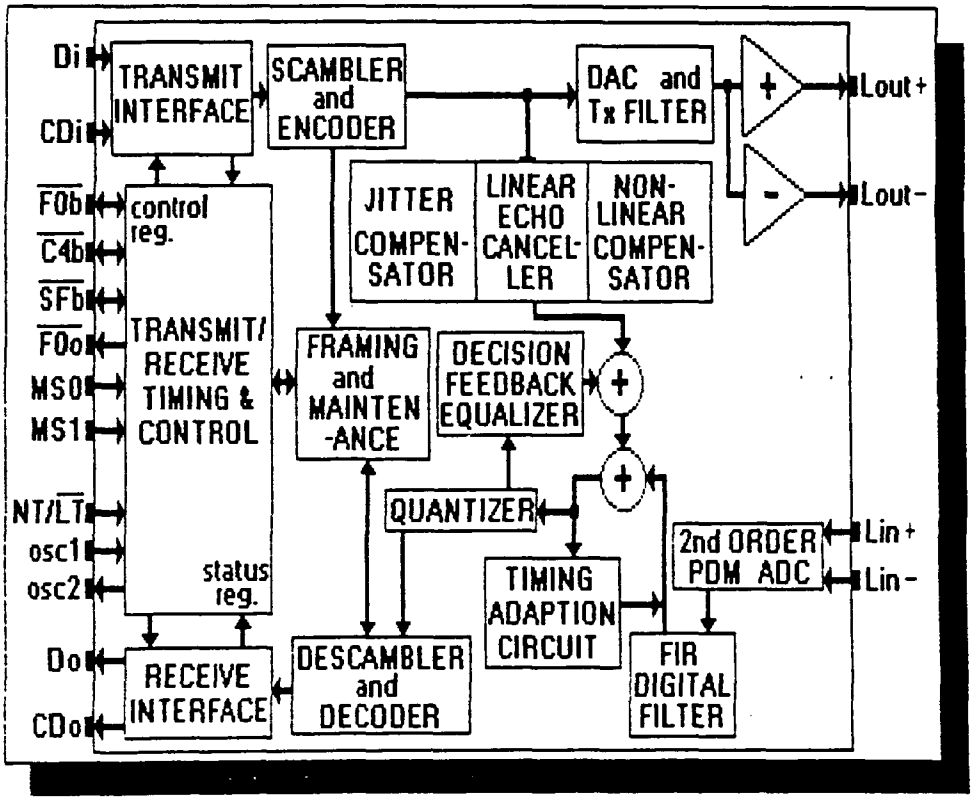


Figure 5.8: MT8910 DSLIC Block Diagram

CONCLUSION

Status of the ISDN Central Office Project

At present the T-Card and U-Card have been built and tested. The Main Switch Card has been revised and was tested in the initial design. However, operation of the switch via the PC was never tested. The overall design, including intercard communication, cannot be adequately tested until the software revision, implementation, and testing has been completed. This includes LAP-D and Q.931 functions and is scheduled as part of a Master of Science thesis project for late 1991.

Interface Capabilities

Presently the design will support up to 128 devices, sixty-four each at the U-Interface and at the S/T-Interface. The main switch provides a potential capacity of 256 channels, but as yet the PRI is inactive. Due to the seperation of functions on specific cards, the capacity could be easily expanded.

Commercial Schematics

Detailed schematics have been developed for all PC boards, in order that the design could be commercially manufactured. The U-Interface's biphase signaling

requires design change implementations to meet CCITT 2B1Q signaling standards.

U-Interface Card Testing

After designing and wirewrapping the U-Card, basic hardware and interface testing was performed primarily in an IBM XT PC as follows:

1. Wirewrap was tested for continuity with an ohm meter.
2. EPROMs were then programmed with assembler test programs, as illustrated in Appendix D.
3. The PC side of the PC interface was tested using the IBM debug software to read from and write to the DP-RAM.
4. The first test program tested EPROM and SRAM chip selects and R/W lines.
5. The next program tested reading from and writing to the DP-RAM via the 6809, using the IBM debug software to read the DP-RAM from the PC side.
6. The third program tested reading from and writing to the SRAM, the DX, the Protocol Controller, and the Interval Timer, as well as the Controller's Abort interrupt writing the results to DP-RAM.
7. The final program tested each of the daisy-chained DNICs, via the DX, and the Interval Timer interrupt. It also tested the MC6809 side of the Dual-Port RAM interrupt, using the fill feature of the debug package.

Diagnostics were performed on each chip on the board. Registers were set in the MT8980 DX and communication with the DNICs was tested via D-channel loopback.

The MT8980 DX also tested the Protocol Controller's Abort interrupt. The timeout timer and its interrupt were tested. The mailbox Dual-Port RAM was tested, as was the interrupt interface between the PC and the MC6809. Test results were written to the Dual-Port RAM and checked by the PC.

Suggested Design Changes

In order to bring the existing design into compliance with CCITT ISDN standards and to adapt this design to the commercialization perspective, several basic changes are required. These not only include changes within specific boards, but also, adding an additional board to further separate the functionality and increase the expandability of the design.

The U-Interface Card

2B1Q Signaling Implementation To implement 2B1Q signaling on the U-Card, a DSLIC, MT8910 Digital Subscriber Line Interface Circuit, would need to replace each DNIC in the existing design. The daisy-chain would need to be rewired, because the DSLIC's pins do not match the DNIC's pins. With the exception of adding a counter to generate the superframe pulse, the remainder of the circuitry could remain the same providing the number of chained devices is not increased. The DSLIC features are:

- CCITT level-1 and level-2 U-Interface standards implementation;
- Loop range of over 5.5 km;
- A minimum of 60dB echo cancellation;

- A 4 kbps M channel for embedded operations channel messages on the 160 kbps, 80 baud line;
- High-performance 2B1Q line code;
- Frame and superframe synchronization;
- Low power consumption of 200 mW;
- Single 5V power supply;

One difference between the pins is the generation of a 12 ms superframe pulse by the DSLIC ($\overline{SFb}$). Replacing the DNICs with DSLICs would require:

1. the addition of a 2V analog power source and ground;
2. and the possible addition of a D-C ST-BUS to the DX in Dual-Port Mode for daisy-chaining up to 16 devices. Sixteen DNICs can also be daisy-chained.

Expansion Card Design Two types of expansion cards are recommended. If traffic projection is light, the existing U-Card design will suffice. However due to the rapidly increasing demands on channel bandwidth, a second type of U-Interface card with either dedicated HDLC Controllers for each DNIC or a reduction in the number of DNICs in a single daisy chain is foreseen. Any DNIC to Controller ratio is possible. and a single MT8980D DX could support at least one additional Controller, with two ST-BUSes interfacing to the connector. One DX can support four dedicated Controllers with four ST-BUSes interfacing to the connector. Identical recommendations apply using DSLICs in place of DNICs.

The Main Switch Card In a large scale implementation, where multiple Primary Rate Interfaces are involved, a separate division of functionality is required. Up to four PRI circuits could be supported by a single DX on the same board, or up to eight could be placed if the DX was moved to a separate board. With the DX on the same board as 4 PRIs, a microprocessor system would need to be included. Both designs would require multiple, microprocessor controlled switches and timing on the Main Switch Card, which would consist of a matrix of DXs. For total seperation of interface functions in a multiple PRI environment, seperation of the PRI and the switching is recommended for all designs. This will enable expanding PRI capabilities by plugging in a few chips.

BIBLIOGRAPHY

[1] Fisher D., Maynard P., and Alexander S. *Broadband ISDN.* Computer Communications, Volume 11. London England: Butterworth and Company, August 1988.

[2] Rowe, Stanford H., II. *Business Telecommunications.* USA: Science Research Associates, Inc., 1988.

[3] Tanenbaum, Andrew S. *Computer Networks.* Englewood Cliffs, NJ: Prentice Hall, 1989.

[4] Stallings, William. *Data and Computer Communications.* New York, NY: Macmillan Publishing Company, 1985.

[5] Venkataraman, Geetha. *Design of a Central Office for an ISDN System.* Master's Thesis, Iowa State University, 1990.

[6] Bradley, Angela M. *Design of a PC-based ISDN Central Office.* Master's Thesis, Iowa State University, 1991.

[7] Rainer, Handel. *Evolution of ISDN Towards Broadband ISDN.* New York, NY: IEEE Network, January 1989.

[8] Stallings, William. *Handbook of Computer-Communications Standards, Volume 1: The Open Systems Interconnection (OSI) Model and OSI-Related Standards.* New York, NY: Macmillan Publishing Company, 1987.

[9] Eggebrect, Lewis C. *Interfacing to the IBM Personal Computer.* Indianapolis, IN: Howard W. Sams and Co., 1990.

[10] *Integrated Device Technology, Inc. Memory Devices.* USA: IDT, Inc. 1990.

[11] *Intel Peripherals.* Mt. Prospect, IL: Intel Corporation, 1989.

[12] *International Telegraph and Telephone Consultative Committee.* Volume 6. Red Book, VIII Plenary Assembly. Malaga: CCITT, 1988.

[13] Krutz, Ronald L. *Interfacing Techniques in Digital Design with Emphasis on Microprocessors* . New York, NY: John Wiley and Sons, 1988.

[14] Stallings, William. *Introduction to ISDN.* New York, NY: Macmillan Publishing Company, 1989.

[15] Habara, Kohei. *ISDN, A Look at the Future Through the Past.* New York, NY: IEEE Communications, January 1988.

[16] Kessler, Gary C. *ISDN: Concepts, Facilities, and Services.* St. Louis, MO: McGraw-Hill, Inc. 1990.

[17] *JDR PR-1 and PR-2 Users Manual.* Los Gatos, CA: JDR Microdevices, 1986.

[18] *MC6809 Preliminary Programming Manual.* Oak Hill, TX: Motorola, Inc., 1979.

[19] *Microelectronics Data Book: Don't Design Without It.* Issue 6, San Diego, CA: Mitel Corporation, 1988.

[20] *Microprocessor, Microcontroller, and Peripheral Data.* Volume 2, Oak Hill, TX: Motorola, Inc., 1988.

[21] *Model 7344 PAL Programmer User Manual.* Bay St. Louis, MS: GTEK, Inc. 1987.

[22] *Model 9000 EPROM Programmer User Manual.* Waveland, MS: GTEK, Inc. 1986.

[23] *Proposed high speed packet switch for broadband integrated networks.* London, England: Butterworth & Co Ltd. Volume 12, Number 6, December, 1989.

[24] *Telephony.* McGraw-Hill Encyclopedia of Science and Technology: Volume 18, 6th Edition, page 172, New York, NY: McGraw-Hill, Inc. 1987.

[25] *Microsoft MS-DOS Version 3 Program Development and Winchester Command Guide* St. Joseph, MI: Zenith Data Systems, 1986.

[26] *The TTL Data Book.* Dallas, TX: Texas Instruments, Inc., 1981.

[27] Pandhi, Sushil N. *The Universal Data Connection.* New York, NY: IEEE Spectrum, July 1987.

[28] Overman, Micheal. *Understanding Communications*. London England: Lutterworth Press, 1974.

APPENDIX A. ACRONYMS

ADPCM	Adaptive Differential Pulse Code Modulation
AMI	Alternating Mark Inversion
ARPA	Advanced Research Projects Agency (of the DOD)
ARPANET	ARPA's Network
ATM	Asynchronous Transfer Mode
AT&T	American Telephone and Telegraph, Inc.
AZI	Alternating Zero Inversion
BCD	Binary Coded Decimal
B-ISDN	Broadband ISDN
bps	bits per second
BRI	Basic Rate Interface (ISDN)
CCIS	International Telegraph and Telephone Consultative
CCITT	International Telegraph and Telephone Consultative Committee
CEPT	Conference of European Postal and Telecommunications Association
CH RDY	Channel Ready
CRC	Cyclic Redundancy Check
CS	Chip Select
DC	Direct Current
DNIC	MT8972 Digital Network Interface Circuit
DP-RAM	Dual-Port Random Access Memory
DOD	(U.S.A.) Department of Defense
DSLIC	MT8910 Digital Subscriber Line Interface Circuit
DTA	Data Transfer Acknowledgement
DX	MT8980 or MT8981 Digital Crosspoint Switch
EOP	End Of Packet (bit sequence)
EPROM	Erasable/Programmable Read Only Memory
FAX	Facsimile
FCC	Federal Commerce Commission
FCS	Frame Check Sequence
FDM	Frequency Division Multiplexing
FIRQ	Fast Interrupt Request

GA	Go-Ahead (bit sequence)
Gbps	Gigabits (or billions of bits) per second
HDLC	High-level Data Link Control
Hz	Hertz (cycles per second)
IBM	International Business Machines, Inc.
I/O	Input/Output
IRQ	Interrupt Request
ISDN	Integrated Services Digital Network
ISN	Integrated Services Network
ISO	International Organization for Standardization
ISPBX	Integrated Services Private Branch eXchange
kbps	Kilobits (thousands of bits) per second
km	Kilometer (thousands of meters)
LAN	Local Area Network
LAPB	Link Access Procedures Balanced (X.25)
LAPD	Link Access Procedures on the D-channel
LE	Local Exchange
LSB	Least Significant Bit (D0)
LT	MITEL – Line Termination
modem	Modulator/demodulator
MRDY	Memory Ready
ms	Milliseconds (thousandths of a second)
MSB	Most Significant Bit (D7)
NMI	Non-Maskable Interrupt
NMOS	n-channel enhancement type transistor
NT	Network Termination equipment
NT1	Network Termination equipment type 1
NT2	Network Termination equipment type 2
NT12	Network Termination equipment (hybrid) types 1 & 2

OSI	Open Systems Interconnection
PABX	Private Automatic Branch Exchange
PAL	Programmable Array Logic
PBX	Private Branch Exchange
PC	Personal Computer
PCM	Pulse Code Modulation
PRI	Primary Rate Interface (ISDN)
PSTN	Public Switched Telephone Network
RAM	Random Access Memory
ROM	Read Only Memory
SAP	Service Access Point
SAPI	Service Access Point Identifier
SNA	Systems Network Architecture (IBM)
SNIC	MT8930 Subscriber Network Interface Circuit
SONET	Synchronous Optical NETwork
SRAM	Static Random Access Memory
SS6	Signaling System number 6
SS7	Signaling System number 7
TA	Terminal Adapter
TCM	Time Compression Multiplexing
TDM	Time Division Multiplexing
TE	Terminal Equipment
TE1	Terminal Equipment type 1 (ISDN)
TE2	Terminal Equipment type 2 (non-ISDN)
TEI	Terminal Endpoint Identifier
TV	Television
US	United States (of America)
USA	United States of America
VLSI	Very Large Scale Integration (circuits/chips)
WAN	Wide Area Network
2B1Q	Two Binary, One Quaternary analog line signaling

APPENDIX B. CCITT I-SERIES RECOMMENDATIONS

I.100 Series: General Structure

Section 1: Frame of I-Series Recommendations - Terminology

I.110 General structure of I-series recommendations
I.111 Relationship with other relevant ISDN recommendations
I.112 Vocabulary of terms for ISDN
I.113 General methods

Section 2: Description of ISDNs

I.120 Integrated services digital networks (ISDNs)
I.121 Broadband aspects of ISDN
I.122 Framework for providing additional packet-mode services

Section 3: General Modeling Methods

I.130 Method of characterization of ISDN services and network capabilities of an ISDN

Section 4: Telecommunication Network and Service Attributes

I:140 Attribute technique for the characterization of telecommunication services supported by an ISDN and network capabilities of an ISDN
I.141 ISDN network charging capabilities attributes

I.200 Series: Service Capabilities

I.200 Guidance to the I-200 series of recommendations

Section 1: Service Aspects of ISDNs

I.210 Principles of telecommunication services supported by an ISDN

Section 2: Common Aspects of Services in an ISDN

I.220 Common dynamic description of basic telecommunication services
I.221 Common specific characteristics of services

Section 3: Bearer Services Supported by an ISDN

I.230 Definition of bearer services
I.231 Circuit-mode bearer services categories
I.232 Packet-mode bearer services

Section 4: Teleservices Supported by an ISDN

I.240 Definition of teleservices
I.241 Teleservices supported by an ISDN

Section 5: Supplementary Services in an ISDN

I.250 Definition of supplementary services
I.251 Number identification supplementary services
I.252 Call offering supplementary services
I.253 Call completion supplementary services
I.254 Multiparty supplementary services
I.255 "Community of interest" supplementary services
I.256 Charging supplementary services
I.257 Additional information transfer supplementary services

I.300 Series: Overall Network Aspects and Functions

Section 1: Network Functional Principles

I.310 ISDN network functional principles

Section 2: Reference Models

I.320 ISDN protocol reference model
I.324 ISDN network architecture
I.325 Reference configurations for ISDN connection types
I.326 Reference configurations for relative network resource requirements
I.32x ISDN hypothetical reference connections (FFS)

Section 3: Numbering, Addressing, and Routing

I.330 ISDN numbering and addressing principles
I.331 Numbering plan for the ISDN era
I.332 Numbering principles for internetworking between an ISDN and a non-ISDN with different numbering
I.333 Terminal selection in ISDN
I.334 Principles to relating ISDN numbers/addresses to OSI reference model network layer addresses
I.335 ISDN routing principles

Section 4: Connection Types

I.340 ISDN connection types

Section 5: Performance Objectives

I.350 General Aspects of Quality of Service and network performance in digital networks, including ISDN
I.351 Recommendations in other Series including network performance objectives that apply at T-reference points of an ISDN
I.352 Network performance objectives for call processing delays

I.400 Series: ISDN User-Network Interfaces

Section 1: ISDN User-Network Interfaces

I.410 General aspects and principles relating to recommendations on ISDN user-network interfaces
I.411 ISDN user-network interfaces - reference configurations
I.412 ISDN user-network interfaces - interface structures and access capabilities

Section 2: Application of I-Series Recommendations to ISDN User-Network Interfaces

I.420 Basic user-network interface
I.421 Primary user-network interface

Section 3: ISDN User-Network Interfaces: Layer 1 Recommendations

I.430 Basic user-network interface - layer 1 recommendations
I.431 Primary user-network interface - layer 1 recommendations
I.43x Higher rate user-network interfaces (FFS)

Section 4: ISDN User-Network Interfaces: Layer 2 Recommendations

I.440 (Q.920) Basic user-network interface data link layer - general aspects
I.441 (Q.921) Primary user-network interface data link layer specification

Section 5: ISDN User-Network Interfaces: Layer 3 Recommendations

I.450 (Q.930) ISDN user-network interface layer – general aspects

I.451	(Q.931)	ISDN user-network interface – specification for basic call control
I.452	(Q.932)	ISDN user-network interface specification - generic procedures for the control of ISDN supplementary services

Section 6: Multiplexing, Rate Adaptation, and Support of Existing Interfaces

I.460		Multiplexing, rate adaption and support of existing services
I.461	(X.30)	Support of X.21, X.21 bis, and X.21 bis based data terminal equipments by an ISDN.
I.462	(X.31)	Support of packet-mode terminal equipment by an ISDN
I.463		Support of data terminal equipments with V-series-type interfaces by an ISDN
I.464		Multiplexing, rate adaption and support of existing interfaces for restricted 64-kb/s transfer capability
I.465		Support by an ISDN of data terminal equipment with V-series type interfaces with the provision for statistical multiplexing

Section 7: Aspects of ISDN Affecting Terminal Requirements

I.470	Relationship of terminal functions to ISDN

I.500 Series: Internetworking Between Various Networks

I.500	ISDN internetworking recommendations
I.510	Definitions and general principles for ISDN internetworking
I.511	ISDN to ISDN layer 1
I.515	Parameter exchange for ISDN internetworking
I.520	General arrangements for network internetworking between ISDNs
I.530	ISDN-PSTN internetworking
I.540	General arrangements for internetworking between circuit switched public data networks and ISDNs for the provision of data transmission

I.550 General arrangements for internetworking between packet switched public data networks and ISDNs for the provision of data transmission

I.560 Requirements to be met in providing the telex service within an ISDN

I.600 Series: Maintenance Principles

I.601 General maintenance principles of ISDN subscriber access and subscriber installation

I.602 Application of maintenance principles to ISDN subscriber installation

I.603 Application of maintenance principles to ISDN basic accesses

I.604 Application of maintenance principles to ISDN primary rate accesses

I.605 Application of maintenance principles to static multiplexed ISDN basic accesses

A.2: OTHER RECOMMENDATIONS RELATED TO ISDN

(C-series) General tariff principles

(D-series) Telephone network and ISDN - Addressing, routing, quality of service, network management, and traffic engineering

(F-series) Telegraph and mobile services

(G-series) International telephone connections and circuits, transmission media, and digital transmission systems

(K-series) Protection against interference

(M-series) General maintenance principles

(P-series) Telephone transmission quality

(Q-series) Telephone switching and signaling

(T-series) Telematic services

(U-series) Telegraph switching

(V-series) Data communication over the telephone network

(X-series) Data communication networks

(Z-series) Functional Specification and Description Language (SDL)

APPENDIX C. U-CARD COMPONENT PIN ASSIGNMENTS

All U-Card major chips' pin assignments are tabularized in this appendix. Each device's table is on a separate page.

Table C.1: MT8910 DSLIC Pin Assignments

PIN#	NAME	DESCRIPTION
1	Lout-	Line Out Minus: 1 of 2 differential output lines for 2B1Q
2	Lout+	Line Out Plus: 1 of 2 differential output lines for 2B1Q
3	AVss	ANALOG GROUND:
4	IC	INTERNAL CONNECTION: Connect to Vss
5	CDSTi	CONTROL/DATA ST-BUS Input: In Dual-Port Mode carries D-C channels; Single-Port Mode goes to Vss
6	DSTi	DATA ST-BUS Input: In Dual-Port Mode carries 2B channels; In Single-Port Mode carries D-C-B-B channels
7	Vss	DIGITAL GROUND:
8	DSTo	DATA ST-BUS Output: In Dual-Port Mode carries 2B channels; In Single-Port Mode carries D-C-B-B channels
9	CDSTo	CONTROL/DATA ST-BUS Output: In Dual-Port Mode carries D-C channels; Single-Port Mode in high-impedance
10	F0od(low)	Delayed Frame Pulse Out: to next daisy-chain device
11	NC	NO CONNECTION:
12-13	MS0-1	MODE SELECT: Selects single or dual port modes and D-C or C-D channel precedence
14	NT/LT(low)	Network/Line Termination: Indicates external/internal timing source
15	IC	INTERNAL CONNECTION: Connect to Vss
16	SFb(low)	Superframe Pulse: 12ms output pulse signifying the start of a superframe
17	C4b(low)	4096kHz CLK (Input in LT mode): two cycles per bit
18	F0b(low)	Frame Pulse (Input in LT mode): ST-BUS frame start 8kHz signal
19	OSC2	Oscillator Output: unused in daisy-chaining
20	OSC1	Oscillator Input: 10.24 MHz C10i input
21	MRST(low)	Master Reset: CMOS input to reset DSLIC
22	Vdd	Digital Power Supply: (+5 Volt)
23	NC	NO CONNECTION:
24	Vdd	Analog Power Supply:
25	Vbias	Bias Voltage: Decouple to AVss through a 1.0 μF capacitor
26	Vref	Reference Voltage: Decouple to AVss through a 1.0 μF capacitor
27	Lin-	Line In Minus: 1 of 2 differential input lines for 2B1Q
28	Lin+	Line In Plus: 1 of 2 differential input lines for 2B1Q

Table C.2: MT8952B HDLC Protocol Controller Pin Assignments

PIN#	NAME	DESCRIPTION
1	TxCEN(low)	Transmit Clock Enable: for external timing mode '1' high impedance: '0' enables transmit section
2	RxCEN(low)	Receive Clock Enable: for external timing mode '1' inhibits clock: '0' enables receive section
3	CDSTo	C and D channel output in ST bus format
4	CDSTi	C and D channel input in ST bus format
5	WD(low)	Watch-Dog timer output: 0-timer times out
6	IRQ(low)	Interrupt request output: flags new HDLC frame and when a go ahead sequence is detected
7-10	A0-A3	Address bit inputs: address various registers
11	CS(low)	Chip Select Input: enables read or write input
12	E	Clock Enable Input: activates address bus and R/W inputs
13	R/W(low)	Read/Write Control: designates operation of the I/O buffer
14	Vss	Ground (0 Volt)
15-22	D0-D7	Data bus I/O ports: interface to the 6809
23	REOP	Receive End Of Packet: signals closing flag
24	TEOP	Transmit End Of Packet: signals when a packet is transmitted or aborted
25	CKi	Bit Rate Clock Input: ST-BUS C4i(low) signal
26	F0i(low)	Frame Pulse Input: ST-BUS frame start and Watch-Dog timer input
27	RST(low)	Schmidt Trigger Input: Resets all registers
28	VDD	Supply (+5 Volt)

Table C.3: MT8972 DNIC Pin Assignments

PIN#	NAME	DESCRIPTION
1	Lout	Line Out: Biphase output referenced to Vbias
2	Vbias	Input Bias Voltage: Decouple to Vdd through a 0.33 μF capacitor
3	Vref	Input Reference Voltage: Decouple to Vdd through a 0.33 μF capacitor
4-6	MS2-0	MODE SELECT: Selects 1 of 9 possible modes
7	RegC	Regulator Control: A 512 kHz CLK
8	(F0/CLD)(low)	Frame Pulse (Input): ST-BUS frame start pulse
9	CDSTi/CDi	Control/DATA ST-BUS Input: Dual-Port Mode carries D-C channels; Single-Port Mode disconnect
10	CDSTo/CDo	Control/DATA ST-BUS Output: Dual-Port Mode carries D-C channels; Single-Port Mode disconnect
11	Vss	DIGITAL GROUND:
12	DSTo/Do	DATA ST-BUS Output: In Dual-Port Mode carries 2B channels In Single-Port Mode carries D-C-B-B channels
13	DSTi/Di	DATA ST-BUS Input: In Dual-Port Mode carries 2B channels In Single-Port Mode carries D-C-B-B channels
14	(F0o/RCK)(low)	Frame Pulse (Output): ST-BUS frame start pulse connected to next DNIC in daisy-chain
15	(C4b/TCK)(low)	Data Clock/Transmit Baud Rate Clock: a 4.096MHz input signal for transmit bit rate
17	C4b(low)	4096kHz CLK (Input in LT mode): 2 cycles/bit
16	OSC2	Oscillator Output: unused in daisy-chaining
17	OSC1	Oscillator Input: 10.24 MHz C10i CMOS input
18-19	NC	NO CONNECTION:
20	TEST	Test Pin: connect to Vss
21	Lin	Line In: Analog biphase input referenced to Vbias
22	Vdd	Digital Power Supply: (+5 Volt)

Table C.4: The MT8980 DX Pin Assignments

PIN#	NAME	DESCRIPTION
1	DTA(low)	Data Acknowlegement (Open Drain Output): pulled low to signal data is processed – requires 909 Ohm resistor
2-9	STi0-STi7	Eight ST-BUS Inputs:
10	VDD	Supply (+5 Volt)
11	F0i(low)	Frame Pulse Input: ST-BUS frame pulse
12	C4i(low)	Bit Rate Clock Input: ST-BUS signal
13-18	A0-A5	Address bit inputs: address internal memories
19	DS	Data Strobe (Input): used for writes
20	R/W(low)	Read/Write:
21	CS(low)	Chip Select:
22-29	D7-D0	Tri-State bidirectional Data Pins:
30	Vss	Ground (0 Volt)
31-38	STo0-STo7	Eight ST-BUS Outputs:
39	ODE	Output Drive Enable: '1' – normal operation '0' – ST-BUSes go to high-impedance
40	CSTo	Control ST-BUS Output: tied in this design

Table C.5: Motorola 6809 Microprocessor Pin Assignments

PIN#	NAME	DESCRIPTION
1	Vss	Ground (0 Volt)
2	NMI(low)	Non-Masked Interrupt:
3	IRQ(low)	Normal Masked Interrupt:
4	FIRQ(low)	Fast Masked Interrupt:
5	BS	C and D channel output in ST bus format
6	BA	C and D channel output in ST bus format
7	Vcc	Ground (0 Volt)
8-23	A0-A15	Address line outputs: address locations in devices on the bus
24-31	D7-D0	Data bus I/O ports: interface to MC6809 bus devices' data ports
32	R/W(low)	Read/Write Control: designates the operation of the I/O buffer
33	(DMA/BREQ)(low)	DMA Bus Request Pin: not used this design
34	E	Clock: signals the start and stop of cycles
35	Q	Clock: signals the start and stop of a valid address cycle
36	MRDY	Memory Ready (Input): suspends the R/W cycle for 10μs maximum when low
37	RESET(low)	Reset Hardware Input: resets entire system
38	EXTAL	Crystal Clock Input:
39	XTAL	Crystal Clock Input:
40	HALT(low)	Internal Software Halt:

Table C.6: The 64k Byte EPROM Pin Assignments

PIN#	NAME	DESCRIPTION
1	A15	Address line input: address memory locations
2	A12	Address line input: address memory locations
3-10	A7-A0	Address line input: address memory locations
11-13	O0-O2	Programming data ports: shunted to Vcc
14	GND	Ground (0 Volt)
15-19	O3-O7	Programming data ports: shunted to Vcc
20	CE(low)	Chip Enable: enables chip ports read oper.
21	A10	Address line input: address memory locations
22	OE(low)/Vpp	Output Enable: valid data strobe
23	A11	Address line input: address memory locations
24-25	A9-A8	Address line input: address memory locations
26-27	A13-A14	Address line input: address memory locations
28	Vcc	Power Supply (+5 Volt)

Table C.7: The 8k Byte SRAM Pin Assignments

PIN#	NAME	DESCRIPTION
1	NC	NO CONNECTION:
2	A12	Address line input: address memory locations
3-10	A7-A0	Address line input: address memory locations
11-13	D0-D2	Data bus I/O ports: interface to MC6809
14	GND	Ground (0 Volt)
15-19	D3-D7	Data bus I/O ports: interface to MC6809
20	CS1(low)	Chip Select: enables chip ports
21	A10	Address line input: address memory locations
22	OE(low)	Output Enable: valid data strobe
23	A11	Address line input: address memory locations
24-25	A9-A8	Address line input: address memory locations
26	CS2	Chip Select: enables chip ports
27	WE(low)	Write Enable: valid data strobe
28	Vcc	Power Supply (+5 Volt)

Table C.8: The 1k Byte Dual-Port RAM Pin Assignments

PIN#	NAME	DESCRIPTION
1-24	LEFT	MC6809 BUS
25-48	RIGHT	PC-BUS
1	CE(low)	Chip Enable: enables chip ports normal oper.
2	R/W(low)	Read/Write:
3	BUSY(low)	Busy Output: signals conflict access denied
4	INT(low)	Interrupt Output: signals mailbox message
5	OE(low)	Output Enable: valid data strobe
6-15	A0-A9	Address line input: address memory locations
16-23	I/O 0-7	Data bus I/O ports: interface to MC6809
24	GND	Ground (0 Volt)
25-32	I/O 0-7	Data bus I/O ports: interface to PC-BUS
33-42	A9-A0	Address line input: address memory locations
43	OE(low)	Output Enable: valid data strobe
44	INT(low)	Interrupt Output: signals mailbox message
45	BUSY(low)	Busy Output: signals conflict access denied
46	R/W(low)	Read/Write:
47	CE(low)	Chip Enable: enables chip ports normal oper.
48	Vcc	Power Supply (+5 Volt)

Table C.9: The 8254 Interval Timer Pin Assignments

PIN#	NAME	DESCRIPTION
1-8	D7-D0	Data bus I/O ports: interface to MC6809
9	CLK0	Clock Input Counter 0:
10	OUT0	Counter 0 Output Strobe:
11	GATE0	Counter 0 Enable/Disable: '1' – enable
12	GND	Ground (0 Volt)
13	GATE1	Counter 1 Enable/Disable: '1' – enable
14	OUT1	Counter 1 Output Strobe:
15	CLK1	Clock Input Counter 1:
16	GATE2	Counter 2 Enable/Disable: '1' – enable
17	OUT2	Counter 2 Output Strobe:
18	CLK2	Clock Input Counter 2:
19-20	A0-A1	Address line input: address registers
21	CS(low)	Chip Select: enables chip ports normal oper.
22	RD(low)	Read Enable:
23	WR(low)	Write Enable:
24	Vcc	Power Supply (+5 Volt)

APPENDIX D. PARTS LISTS

Main Card Parts List

U-Interface Card Parts List

External Board Parts List

Table D.1: Main Card Components

QTY	SOCKET SIZE	DEVICE NAME	DESCRIPTION
1	—	PC board	IBM compatible board
1	24	MT8940	T1/CEPT Digital Trunk PLL
1	40	MH89760	ESF Digital Trunk Interface
1	40	MT8980D	Digital Time/Space Crosspoint Switch
1	14	SN7400	Quad 2-Input NAND Gate
1	14	SN7402	Quad 2-Input NOR Gate
1	14	SN7408	Quad 2-Input AND Gate
1	16	SN74LS85	4-bit Magnitude Comparator
1	14	SN7486	Quad 2-Input XOR Gate
1	16	SN74LS138	3 to 8 Demultiplexer
1	16	SN74LS163	Synchronous 4-bit Counter
2	20	SN74LS244	Octal Buffers/Line Drivers
1	20	SN74LS245	Octal Bus Transceiver
1	14	SN74LS624	Voltage Controlled Oscillator
1	—		12.355MHz Crystal
1	—		16.388MHz Crystal
1	—	Connector	26 Pin Ribbon (ST-BUS)
1	—	Resistor	909 Ohm 0.25W
1	—	Resistor	10k Ohm
2	—	Resistor	4.7k Ohm
1	—	Capacitor	33pF
1	—	Capacitor	56pF
2	—	Capacitor	10μF
5	—	Capacitor	0.1F (bypass)
1	—	Dip Switch	8 position

Table D.2: S/T-Card Components

QTY	SOCKET SIZE	DEVICE NAME	DESCRIPTION
1	—	PC board	IBM compatible board
8	28	MT8930	Subscriber Network Interface Circuit
1	40	MC6809	Motorola 8-bit microprocessor
1	48	IDT7130SA	8x1k Dual-Port RAM
1	28	INTEL27512	8x64k EPROM
1	28	INTEL5164S	8x8k SRAM (Hitachi 6264)
1	20	16L8 PAL	(Programmable Array Logic)
1	28	INTEL8259A	Interrupt Controller
1	14	SN7400	Quad 2-Input NAND Gate
1	14	SN7402	Quad 2-Input NOR Gate
1	14	SN7404	Hex Inverter
1	14	SN5407	Hex Buffer/Driver
1	14	SN7408	Quad 2-Input AND Gate
1	14	SN7430	8-Input AND Gate
1	14	SN7432	Quad 2-Input OR Gate
1	16	SN74LS85	4-bit Magnitude Comparator
2	14	SN7486	Quad 2-Input XOR Gate
2	20	SN74LS244	Octal Buffers/Line Drivers
4	20	SN74LS245	Octal Bus Transceivers
2	16	SN74LS138	3 to 8 Line Demultiplexers
1	—	XTAL	4.0MHz Crystal
1	—	Connector	26 Pin Ribbon (ST-BUS)
12	—	Resistor	910 Ohm (Pullup)
10	—	Capacitor	10μF
5	—	Capacitor	0.1F (bypass)
2	—	Capacitor	18pF (XTAL crystal)
2	—	Resistor	4.7k Ohm

Table D.3: U-Card Components

QTY	SOCKET SIZE	DEVICE NAME	DESCRIPTION
1	—	PC board	IBM compatible board
1	28	MT8952	HDLC Protocol Controller
8	22	MT8972	Digital Network Interface Circuit
1	40	MT8980D	Digital Time/Space Crosspoint Switch
1	40	MC6809	Motorola 8-bit microprocessor
1	48	IDT7130SA	8x1k Dual-Port RAM
1	28	INTEL27512	8x64k EPROM
1	28	INTEL5164S	8x8k SRAM (Hitachi 6264)
1	20	16L8 PAL	(Programmable Array Logic)
1	24	INTEL8254	Interval Timer
1	14	SN7400	Quad 2-Input NAND Gate
1	14	SN7402	Quad 2-Input NOR Gate
2	14	SN7404	Hex Inverters
1	14	SN5407	Hex Buffer/Driver
1	14	SN7430	8-Input AND Gate
2	14	SN7432	Quad 2-Input OR Gate
1	14	SN7486	Quad 2-Input XOR Gate
2	20	SN74LS244	Octal Buffers/Line Drivers
1	20	SN74LS245	Octal Bus Transceiver
1	—	XTAL	4.0MHz Crystal
1	—	Connector	26 Pin Ribbon (ST-BUS)
5	—	Resistor	910 Ohm (Pullup)
6	—	Capacitor	0.1F (bypass)
2	—	Capacitor	18pF (XTAL crystal)
2	—	Capacitor	10μF
16	—	Capacitor	0.33μF

Table D.4: External Components

QTY	DEVICE NAME	DESCRIPTION
1	PC board	
16	Resistor	910 Ohm
16	Capacitor	10μF
16	Capacitor	0.33μF
16		2 to 1 Transformers

APPENDIX E. PAL AND CIRCUIT TEST PROGRAMMING

PAL Programming and Generated Files

PAL Program

```
PAL16L8 J5
U000 TIMOTHY TOILLION 6-21-91
ADDRESS DECODER FOR CHIP SELECT
ISU
PIN1 E Q A10 A15 A14 A13 A12 A11 GND
PIN11 PIN12 PIN13 INTT DX HDLC DPRAM SRAM EPROM VCC

IF (VCC) /SRAM = /A15 * /A14 * /A13 * E
           + /A15 * /A14 * /A13 * Q
IF (VCC) /DPRAM = /A15 * /A14 * A13 * /A12 */A11 * E
           + /A15 * /A14 * A13 * /A12 */A11 * Q
IF (VCC) /DX = /A15 * /A14 * A13 * A12 * /A11 * E
           + /A15 * /A14 * A13 * A12 * /A11 * Q
IF (VCC) /HDLC = /A15 * /A14 * A13 * /A12 * A11 * E
           + /A15 * /A14 * A13 * /A12 * A11 * Q
IF (VCC) /INTT = /A15 * /A14 * A13 * A12 * A11 * E
           + /A15 * /A14 * A13 * A12 * A11 * Q
IF (VCC) /EPROM = A14 * E + A15 * E
           + A14 * Q + A15 * Q

FUNCTION TABLE
A15 A14 A13 A12 A11 EPROM SRAM DPRAM HDLC DX INTT
----------
H L X X X L X X X X X
L H X X X L X X X X X
L L L X X X L X X X X
L L H L L X X L X X X
```

```
L L H L H X X X L X X
L L H H L X X X X L X
L L H H H X X X X X L
----------
DESCRIPTION
```

PAL JED File

```
PAL16L8 J5
U000 TIMOTHY TOILLION 6-21-91
ADDRESS DECODER FOR CHIP SELECT
ISU
*MJ**G0*F0*
L0000 11111111111111111111111111111111*
L0032 01111111111111110111111111111111*
L0064 01111111111101111111111111111111*
L0096 11110111111111111011111111111111*
L0128 11110111111110111111111111111111*
L0256 11111111111111111111111111111111*
L0288 01111111111110111011011011111111*
L0320 11110111111110111011011011111111*
L0512 11111111111111111111111111111111*
L0544 01111111111110111011011110111011*
L0576 11110111111110111011011110111011*
L0768 11111111111111111111111111111111*
L0800 01111111111110111011011110110111*
L0832 11110111111110111011011110110111*
L1024 11111111111111111111111111111111*
L1056 01111111111110111011011101111011*
L1088 11110111111110111011011101111011*
L1280 11111111111111111111111111111111*
L1312 01111111111110111011011101110111*
L1344 11110111111110111011011101110111*
V0001 XXXX1OXXXNXXXXXXXXLN*
V0002 XXXXO1XXXNXXXXXXXXLN*
V0003 XXXXOOOXXNXXXXXXXLXN*
V0004 XXXXOO1OONXXXXXXLXXN*
V0005 XXXXOO1O1NXXXXXLXXXN*
V0006 XXXXOO11ONXXXXLXXXXN*
V0007 XXXXOO111NXXXLXXXXXN*
```

PAL Plot File

```
PAL16L8 J5
U000 TIMOTHY TOILLION 6-21-91
ADDRESS DECODER FOR CHIP SELECT
ISU

 0 ---- ---- ---- ---- ---- ---- ---- ----
 1 X--- ---- ---- ---- X--- ---- ---- ----
 2 X--- ---- ---- X--- ---- ---- ---- ----
 3 ---- X--- ---- ---- X--- ---- ---- ----
 4 ---- X--- ---- X--- ---- ---- ---- ----

 8 ---- ---- ---- ---- ---- ---- ---- ----
 9 X--- ---- ---- -X-- -X-- -X-- ---- ----
10 ---- X--- ---- -X-- -X-- -X-- ---- ----

16 ---- ---- ---- ---- ---- ---- ---- ----
17 X--- ---- ---- -X-- -X-- X--- -X-- -X--
18 ---- X--- ---- -X-- -X-- X--- -X-- -X--

24 ---- ---- ---- ---- ---- ---- ---- ----
25 X--- ---- ---- -X-- -X-- X--- -X-- X---
26 ---- X--- ---- -X-- -X-- X--- -X-- X---

32 ---- ---- ---- ---- ---- ---- ---- ----
33 X--- ---- ---- -X-- -X-- X--- X--- -X--
34 ---- X--- ---- -X-- -X-- X--- X--- -X--

40 ---- ---- ---- ---- ---- ---- ---- ----
41 X--- ---- ---- -X-- -X-- X--- X--- X---
42 ---- X--- ---- -X-- -X-- X--- X--- X---

NUMBER OF BLOWN FUSES = 576
```

Circuit Test Programs

SRAM and EPROM Pin Test

```
   ORG   $8000    ; load code starting at this address
START
   LDU   #$1F00   ; create user stacks
   LDS   #$1FFF
LOOP
   LDA   $0000    ; test EPROM and RAM chip selects
   STA   $1000    ; also tests read and write pin signals
   JMP   LOOP

IRQ_ISR
   RTI            ; dummy interrupt routines
FIRQ_ISR
   RTI
NMI_ISR
   LDA   $23FE
   RTI

   ORG   $FFF8      ; load interrupt routine pointers to table
   DW    FIRQ_ISR
   DW    IRQ_ISR
   DW    NMI_ISR
VEC   DW   START

   END
```

DP-RAM Test

```
   ORG   $8000
START             ; setting up stacks
   LDU   #$1F00   ; point to address 1F00 U stack    SRAM
   LDS   #$1FFF   ; point to address 1FFF S stack    SRAM
   LDA   $23FE    ; clearing initial DP-RAM interrupt    Read mailbox

                  ;test DP-RAM
```

```
   LDA   #$00     ; set starting point to test DP-RAM and bus lines
   LDX   #$2000   ; point to starting address DP-RAM
   LDY   #$23FF   ; point to ending address DP-RAM
LOOP1
   STA   ,X+      ; write test to DPRAM and increment address location
   INCA           ; increment value of next byte to be written
   CMP   X,Y      ; last address to write to?
   BNE   LOOP1    ; NO then write to next address
LOOP2
   LDA   $0000    ; test EPROM and RAM chip selects
   STA   $1000    ; also tests read and write pin signals
   JMP   LOOP2

IRQ_ISR
   RTI            ; dummy interrupt routines
FIRQ_ISR
   RTI
NMI_ISR
   LDA   $23FE
   RTI

   ORG   $FFF8     ; load interrupt routine pointers to table
   DW    FIRQ_ISR
   DW    IRQ_ISR
   DW    NMI_ISR
VEC   DW   START

   END
```

Switch, Controller, Timer and HDLC Interrupt Test

```
   ORG   $8000
START              ; setting up stacks
   LDU   #$1F00    ; point to address 1F00 U stack    SRAM
   LDS   #$1FFF    ; point to address 1FFF S stack    SRAM
   LDA   $23FE     ; clearing initial DP-RAM interrupt    Read mailbox
```

```
                    ;initialize DP-RAM

    LDA    #$FF     ; set value to fill DP-RAM
    LDX    #$2000   ; point to starting address DP-RAM
    LDY    #$23FF   ; point to ending address DP-RAM
LOOP1
    STA    ,X+      ; write pattern to DPRAM and increment address location
    CMP    X,Y      ; last address to write to?
    BNE    LOOP1    ; NO then write to next address

    LDX    #$2000   ; point to starting address DP-RAM
    LDY    #$2300   ; point to ending test results address DP-RAM
LOOP2
                    ;test Interval Timer

    LDA    #$21     ; set to write to counter 0 low byte value 0010 0001
    STA    $3C03    ; Write to Timer ControlReg
    STA    $3C00    ; set counter 0 low byte <to 65 decimal>
    LDA    #$22     ; set to write to counter 0 high byte
    LDB    #$00     ; set counter 0 high byte value 0000 0000
    STA    $3C03    ; Write to Timer ControlReg
    STB    $3C00    ; set counter 0 high byte
    LDA    #$21     ; set to write to counter 0 low byte
    STA    $3C03    ; clearing initial Timer interrupt
    LDB    $3C00    ; read counter 0
    STB    ,X+      ; write test to DPRAM and increment address location

                    ;test Switch R/W

    LDA    #$5A     ; set DX CR bits to R/W 0101 1010
    STA    $3800    ; set Control Register    - tests DX WRITE
    LDB    $3828    ; read channel 8 - tests DX Read
    STB    ,X+      ; write test to DPRAM and increment address location

                   ; test 8952's  interrupts -- ABORT

    LDA    #$61    ; set HDLC,s TimingReg to 2-bit D channel 0  0110 0001
    STA    $3005   ; set Protocol Controller        WRITE
    STA    $3005   ; set Protocol Controller        WRITE
```

```
   LDA   #$C0    ; set HDLC,s Control Reg to enable Xmit/Rcv 1100 0000
   STA   $3002   ; set Protocol Controller        WRITE

   LDA   #$90    ; set HDLC,s InterruptReg to enable GA/Abort 1001 0000
   STA   $3007   ; set Protocol Controller        WRITE

   LDA   #$C3    ; set DX CR bits to Write to CMhigh STBUS 3 1100 0011
   STA   $3800   ; set Switch Control Register    WRITE

   LDA   #$FF    ; Load Abort sequence - test HDLC Controller interrupt
   LDB   #$01    ; Load 2 digits of GA sequence
   STA   $3830   ; for channel 0      D channel   WRITE
   STA   $3830   ; for channel 0      D channel   WRITE
   STA   $3830   ; for channel 0      D channel   WRITE
   STA   $3830   ; for channel 0      D channel   WRITE

                 ;test HDLC R/W


   LDA   #$00    ; disable HDLC Protocol Controller
   STA   $3002   ; set HDLC CR - tests Write
   LDB   $3002   ; set HDLC CR - tests Read
   STB   ,X+     ; write test to DPRAM and increment address location

   CMP   X,Y     ; last address to write to?
   BNE   LOOP2   ; NO then write to next address

   LDX   #$2000  ; point to starting address DP-RAM
   JMP   LOOP2

IRQ_ISR
   LDA   #$AA    ; distinguishing value for Controller
   STA   ,X+     ; write test to DPRAM and increment address location
   RTI
FIRQ_ISR
   LDA   #$21    ; set to write to counter 0 low byte
   STA   $3C03   ; clearing initial Timer interrupt
   STA   $200E   ; write test to DPRAM
   LDA   #$BB    ; distinguishing value for Timer
   STA   ,X+     ; write test to DPRAM and increment address location
```

```
   RTI
NMI_ISR
   LDA   $23FE
   LDA   #$CC     ; distinguishing value for DP-RAM
   STA   ,X+      ; write test to DPRAM and increment address location
   RTI

   ORG   $FFF8    ; load interrupt routine pointers to table
   DW    FIRQ_ISR
   DW    IRQ_ISR
   DW    NMI_ISR
VEC   DW   START

   END
```

Daisy-Chain DNIC and Interrupt Tests

```
   ORG   $8000     ; load program at this address
START              ; setting up stacks
   LDU   #$1F00    ; point to address 1F00 U stack    SRAM
   LDS   #$1FFF    ; point to address 1FFF S stack    SRAM
   LDA   $23FE     ; clearing initial DP-RAM interrupt    Read mailbox
   LDD   #$3E 8
   LDD   $8004     ; 1000 x 4 cycles

                   ;initialize DP-RAM

   LDA   #$FF      ; set value to fill DP-RAM
   LDX   #$2000    ; point to starting address DP-RAM
   LDY   #$23FF    ; point to ending address DP-RAM
LOOP1
   STA   ,X+      ; write pattern to DPRAM and increment address location
   CMP   X,Y      ; last address to write to?
   BNE   LOOP1    ; NO then write to next address

                   ; speedup convergence
```

```
   LDA   #$C2     ; set DX CR bits to bcast all \& read STBUS 2 1100 0010
   STA   $3800    ; set Switch Control Register    WRITE

   LDA   #$21     ; set DNIC CR bits to speedup convergence 0100 1000
   STA   $3821    ; for channel 1   WRITE
   STA   $3825    ; for channel 5
   STA   $3829    ; for channel 9
   STA   $382D    ; for channel 13
   STA   $3831    ; for channel 17
   STA   $3835    ; for channel 21
   STA   $3839    ; for channel 25

                  ; setup timer to test interrupt later

   LDA   #$21     ; set to write to counter 0 low byte value 0010 0001
   STA   $3C03    ; Write to Timer ControlReg
   STA   $3C00    ; set counter 0 low byte <to 65 decimal>
   LDA   #$22     ; set to write to counter 0 high byte
   LDB   #$00     ; set counter 0 high byte value 0000 0000
   STA   $3C03    ; Write to Timer ControlReg
   STB   $3C00    ; set counter 0 high byte
   LDA   #$21     ; set to write to counter 0 low byte
   STA   $3C03    ; clearing initial Timer interrupt

                  ; test 8972's set each DNIC's control register loopback

   LDA   #$C2     ; set DX CR bits to bcast all \& read STBUS 2 1100 0010
   STA   $3800    ; set Switch Control Register    WRITE

   LDX   #$2001   ; point to starting test result address DP-RAM
   LDB   #$26     ; set DNIC DiagReg bits to STBUS loopback 0100 0101
   LDA   #$01     ; set DNIC ID
   STA   $3820    ; for channel 0
   STB   $3821    ; for channel 1   loopback
   LDA   #$00     ; set register
   LDB   #$80     ; set register 128 x 4 cycles
LOOP2
   INCA           ; increment register
   CMP   A,B      ; next frame?
   BNE   LOOP2
```

```
   LDA   #$02     ; set DNIC ID
   LDB   $3820    ; read D channel loopback
   STB   ,X+      ; Write D channel loopback to shared memory DP-RAM
   LDB   #$26     ; set DNIC DiagReg bits to STBUS loopback 0100 0101
   STA   $3824    ; for channel 4
   STB   $3825    ; for channel 5
   LDA   #$00     ; set register
   LDB   #$80     ; set register 128 x 4 cycles
LOOP3
   INCA           ; increment register
   CMP   A,B      ; next frame?
   BNE   LOOP3

   LDB   $3824    ; read D channel loopback
   STB   ,X+      ; Write D channel loopback to shared memory DP-RAM
   LDA   #$03     ; set DNIC ID
   LDB   #$46     ; set DNIC DiagReg bits to STBUS loopback 0100 0101
   STA   $3828    ; for channel 8
   STB   $3829    ; for channel 9
   LDA   #$00     ; set register
   LDB   #$80     ; set register 128 x 4 cycles
LOOP4
   INCA           ; increment register
   CMP   A,B      ; next frame?
   BNE   LOOP4

   LDB   $3828    ; read D channel loopback
   STB   ,X+      ; Write D channel loopback to shared memory DP-RAM
   LDA   #$04     ; set DNIC ID
   LDB   #$46     ; set DNIC DiagReg bits to STBUS loopback 0100 0101
   STA   $382C    ; for channel 12
   STB   $382D    ; for channel 13
   LDA   #$00     ; set register
   LDB   #$80     ; set register 128 x 4 cycles
LOOP5
   INCA           ; increment register
   CMP   A,B      ; next frame?
   BNE   LOOP5
```

```
   LDB   $382C    ; read D channel loopback
   STB   ,X+      ; Write D channel loopback to shared memory DP-RAM
   LDA   #$05     ; set DNIC ID
   LDB   #$46     ; set DNIC DiagReg bits to STBUS loopback 0100 0101
   STA   $3830    ; for channel 16
   STB   $3831    ; for channel 17
   LDA   #$00     ; set register
   LDB   #$80     ; set register 128 x 4 cycles
LOOP6
   INCA           ; increment register
   CMP   A,B      ; next frame?
   BNE   LOOP6

   LDB   $3830    ; read D channel loopback
   STB   ,X+      ; Write D channel loopback to shared memory DP-RAM
   LDA   #$06     ; set DNIC ID
   LDB   #$46     ; set DNIC DiagReg bits to STBUS loopback 0100 0101
   STA   $3834    ; for channel 20
   STB   $3835    ; for channel 21
   LDA   #$00     ; set register
   LDB   #$80     ; set register 128 x 4 cycles
LOOP7
   INCA           ; increment register
   CMP   A,B      ; next frame?
   BNE   LOOP7

   LDB   $3834    ; read D channel loopback
   STB   ,X+      ; Write D channel loopback to shared memory DP-RAM
   LDA   #$07     ; set DNIC ID
   LDB   #$46     ; set DNIC DiagReg bits to STBUS loopback 0100 0101
   STA   $3838    ; for channel 24
   STB   $3839    ; for channel 25
   LDA   #$00     ; set register
   LDB   #$80     ; set register 128 x 4 cycles
LOOP8
   INCA           ; increment register
   CMP   A,B      ; next frame?
   BNE   LOOP8

   LDB   $3838    ; read D channel loopback
```

```
   STB    ,X+      ; Write D channel loopback to shared memory DP-RAM

                   ; Test for Interval Timer interrupt

   LDB    $02      ; set for three frame pulses
   STB    $3C00    ; Write counter 0


LOOP9              ; test EPROM and RAM
   LDA    $0000    ; read address 0
   INCA
   STA    $0000    ; write address 0
   JMP    LOOP9

FIRQ_ISR           ; ISR for Interval Timer interrupt
   LDA    #$21     ; set to write to counter 0 low byte
   STA    $3C03    ; clearing Timer interrupt    Write ControlReg
   STA    $200D    ; write test results to DPRAM
   RTI
IRQ_ISR            ; ISR for HDLC interrupts
   LDA    $3006    ; Read Interrupt Flag Reg -- clears GA sequence
   LDA    $3008    ; Read General Status Reg -- clears abort sequence
   STA    $200E    ; write test results to DPRAM
   RTI
NMI_ISR            ; ISR for DP-RAM interrupt
   LDA    $23FE    ; read mailbox to clear interrupt
   STA    $200F    ; write test results to DPRAM
   RTI


   ORG    $FFF8
   DW     FIRQ_ISR
   DW     IRQ_ISR
   DW     NMI_ISR
VEC   DW   START

   END
```

APPENDIX F. U-CARD SCHEMATICS

Gate to Chip Schematics

PC Board Schematics

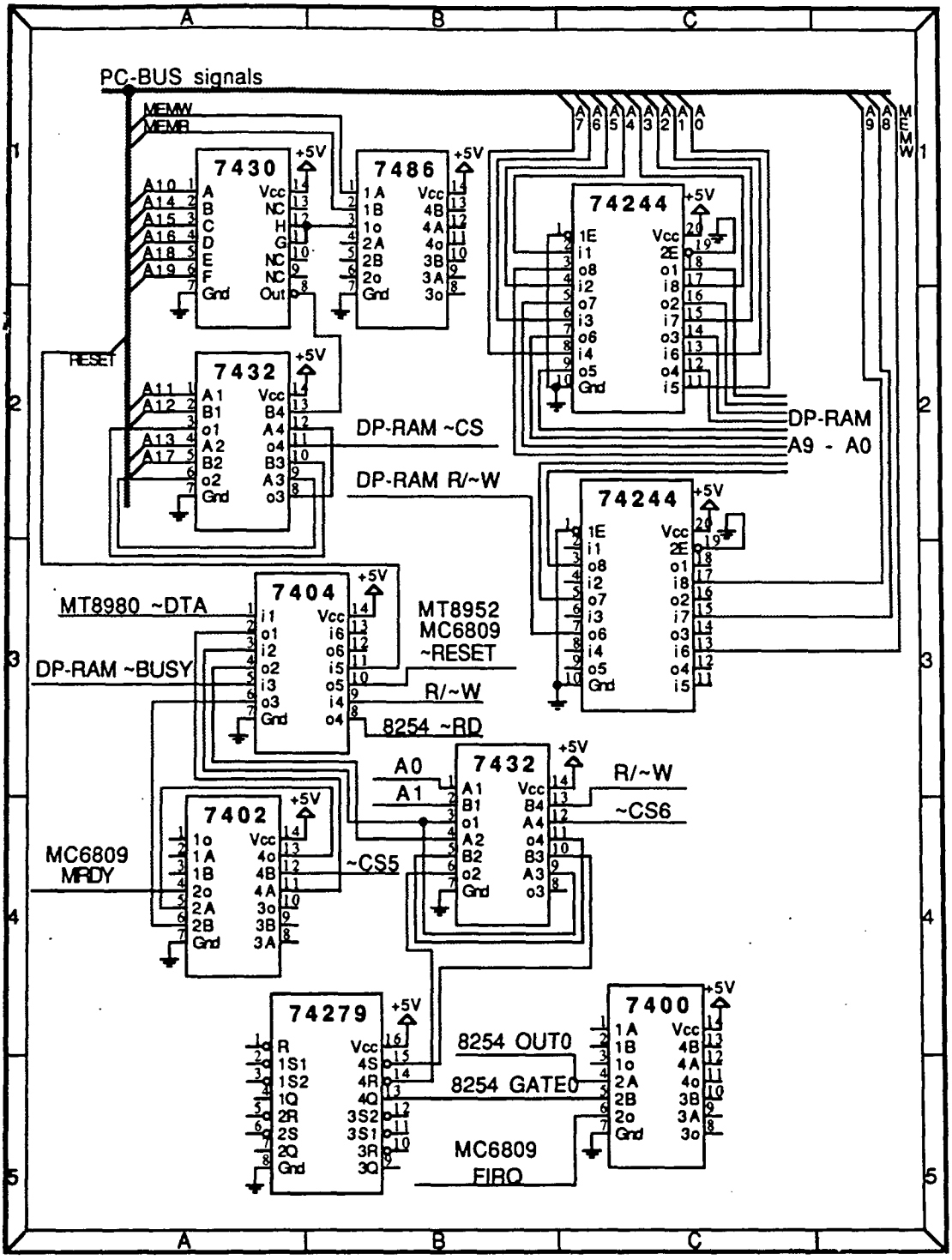
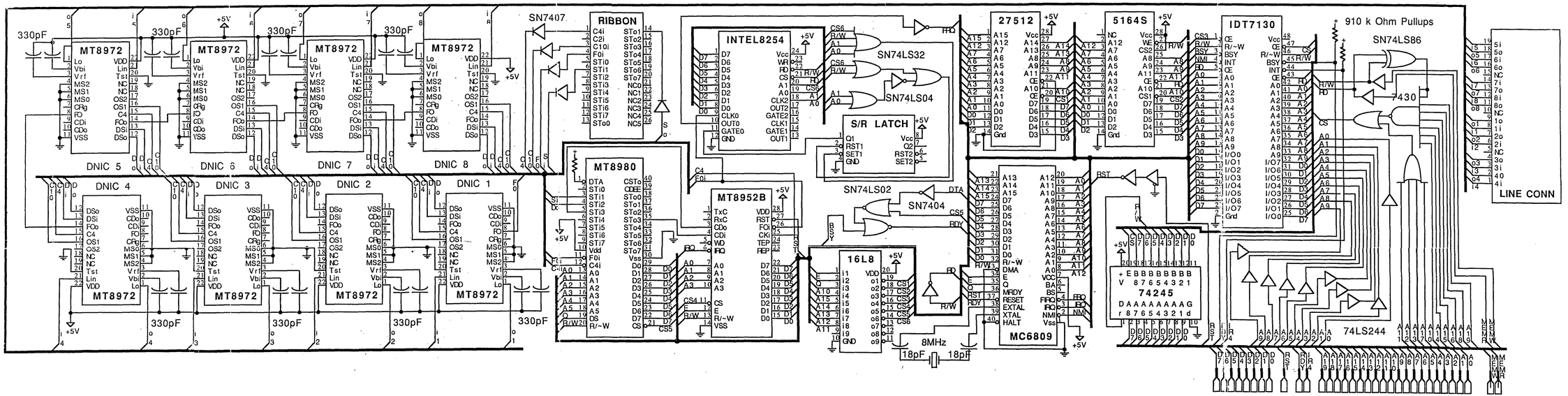


Figure F.1: U-Card Latch and Other Logic


330pF
MT8972
DNIC 5
DNIC 6
DNIC 7
DNIC 8
DNIC 4
DNIC 3
DNIC 2
DNIC 1
+5V
SN7407
RIBBON
MT8980
INTEL8254
MT8952B
S/R LATCH
SN74LS32
SN74LS04
SN74LS02
SN7404
16L8
8MHz
18pF
27512
5164S
IDT7130
910 k Ohm Pullups
SN74LS86
7430
74LS244
MC6809
LINE CONN